

Fig. 1

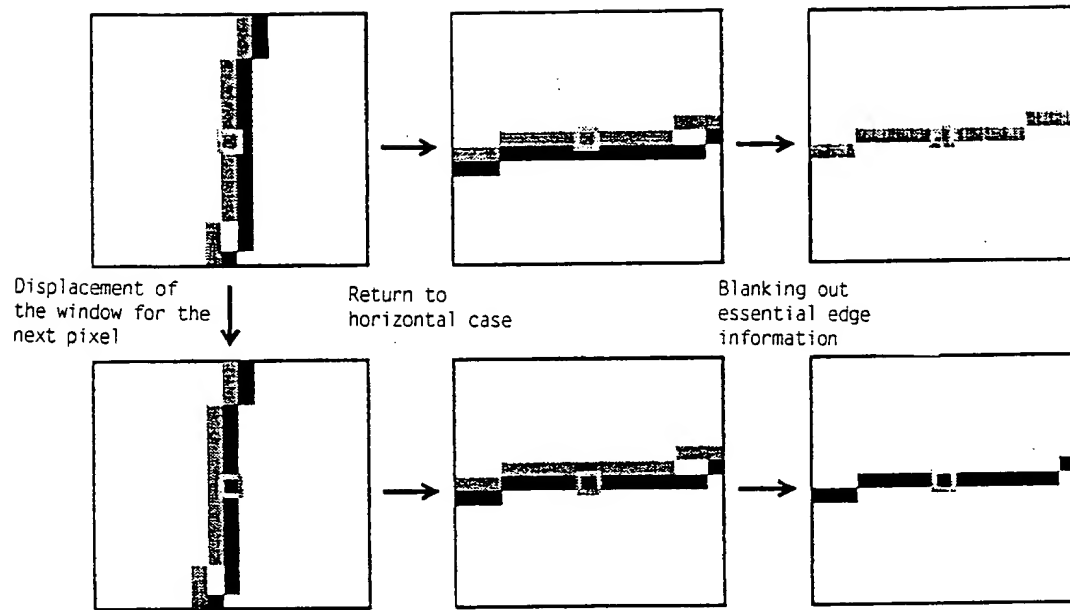


Fig. 2

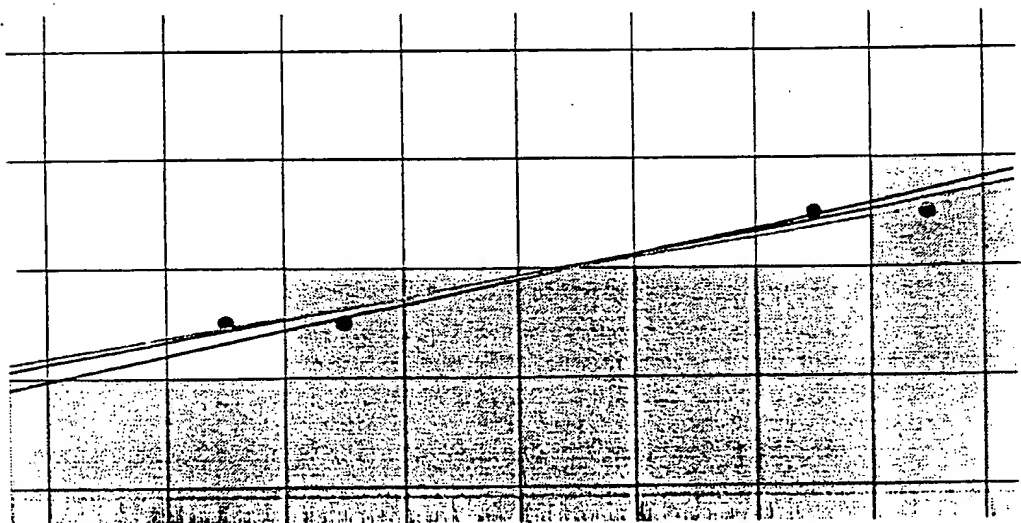


Fig. 3

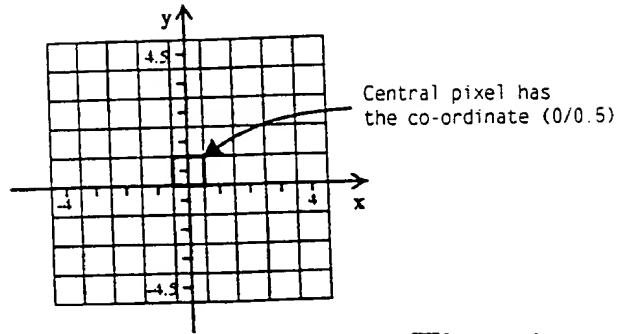


Fig. 4

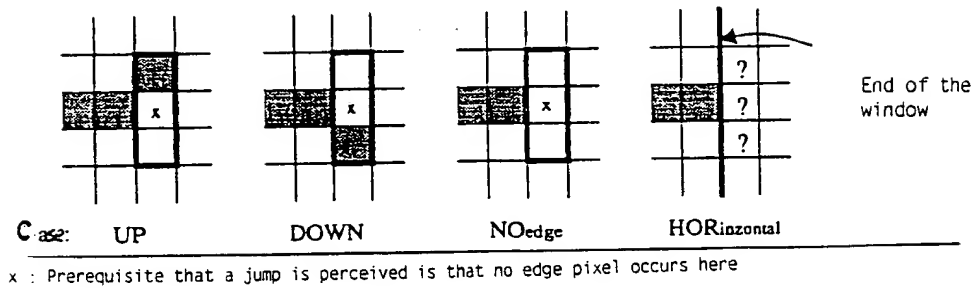


Fig. 5

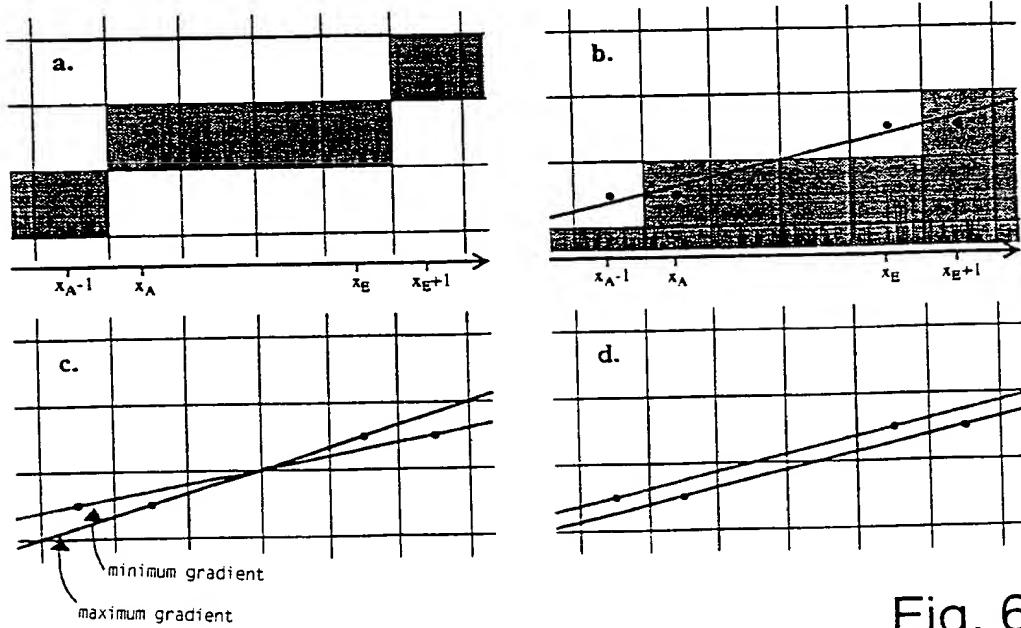


Fig. 6

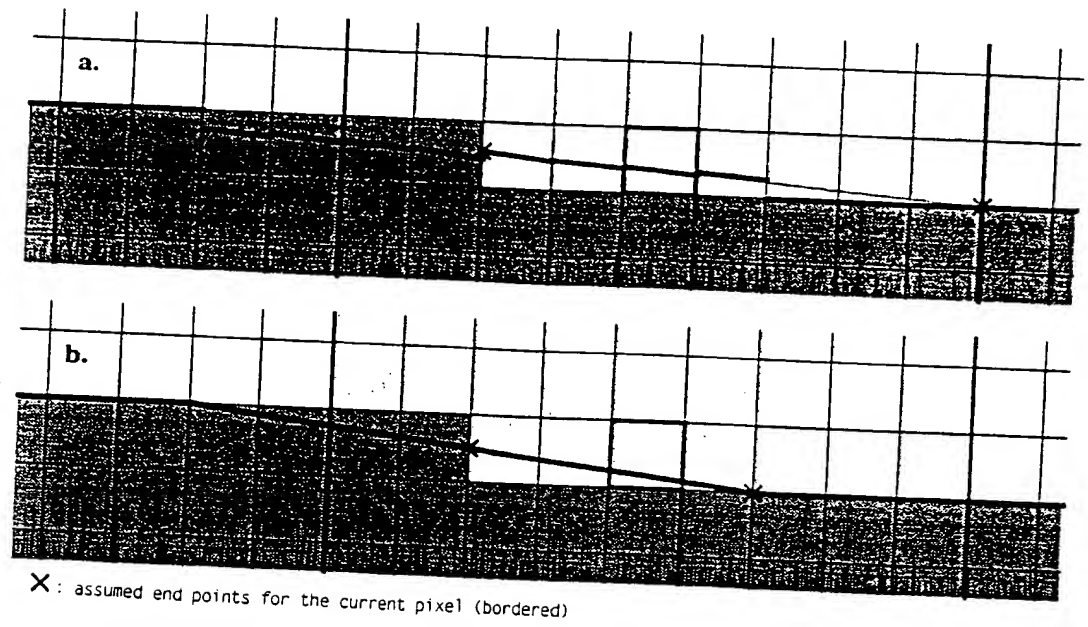


Fig. 7

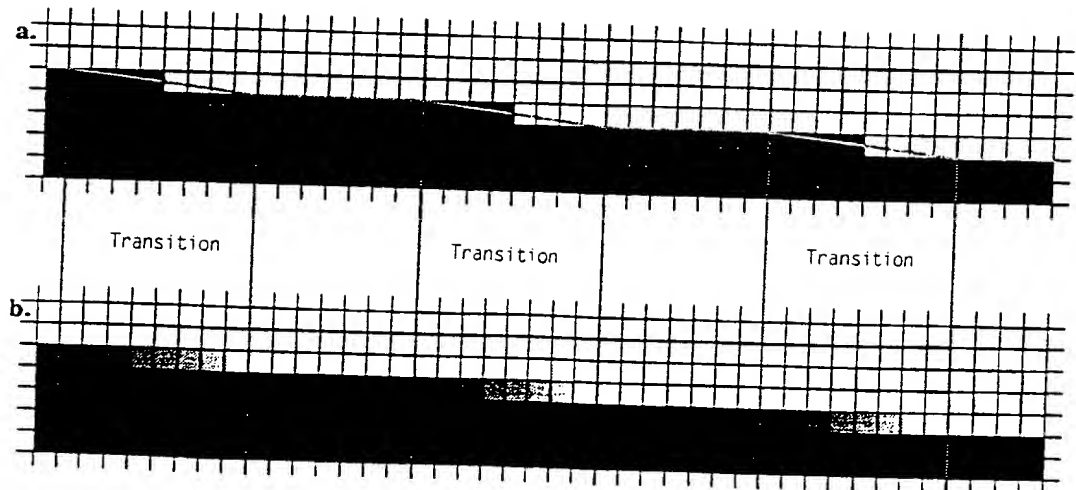


Fig. 8

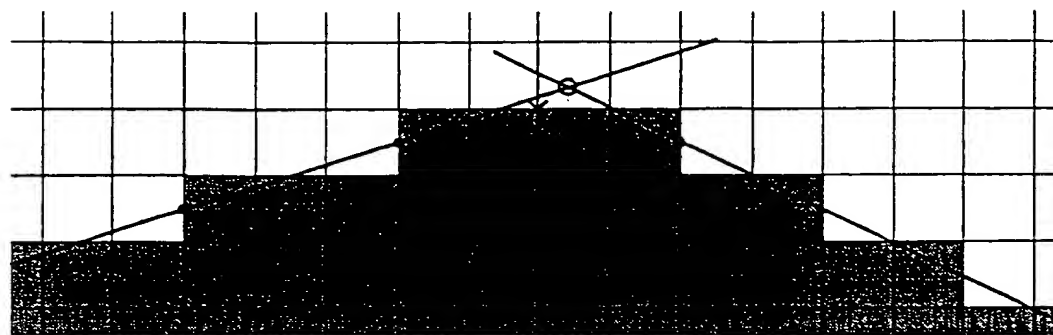


Fig. 9

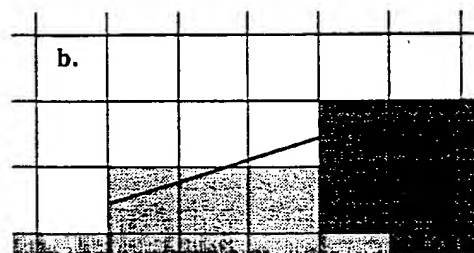
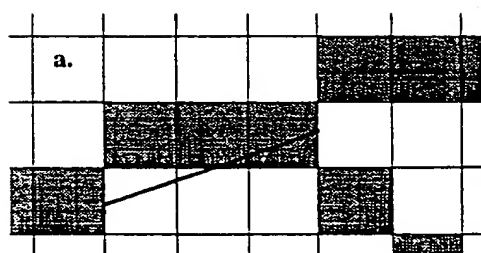
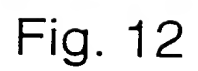
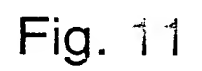


Fig. 10



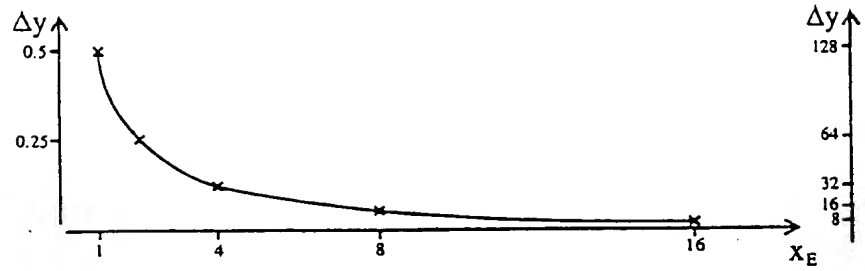


Fig. 13

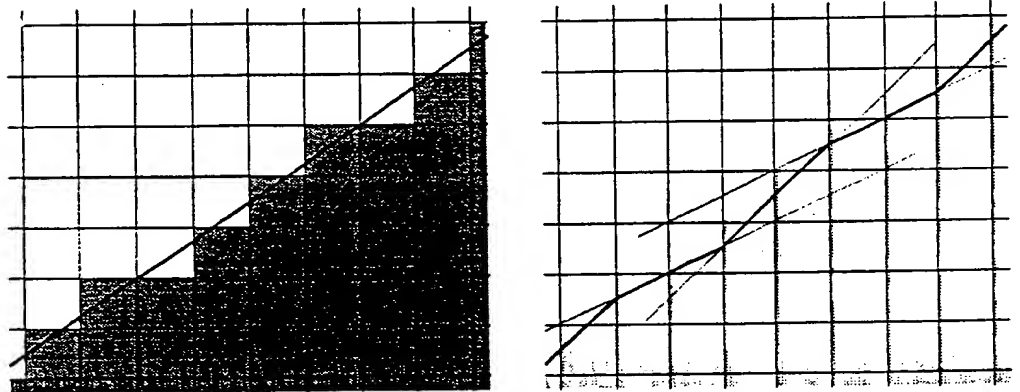
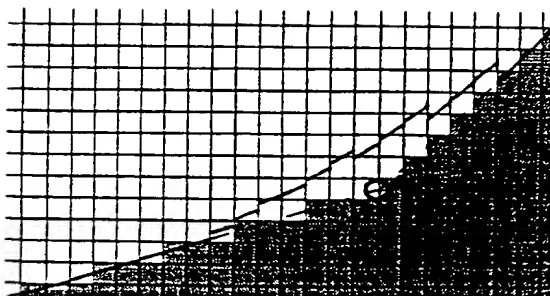


Fig. 14



Corner point not
considered at the
transition of two edges

Fig. 16

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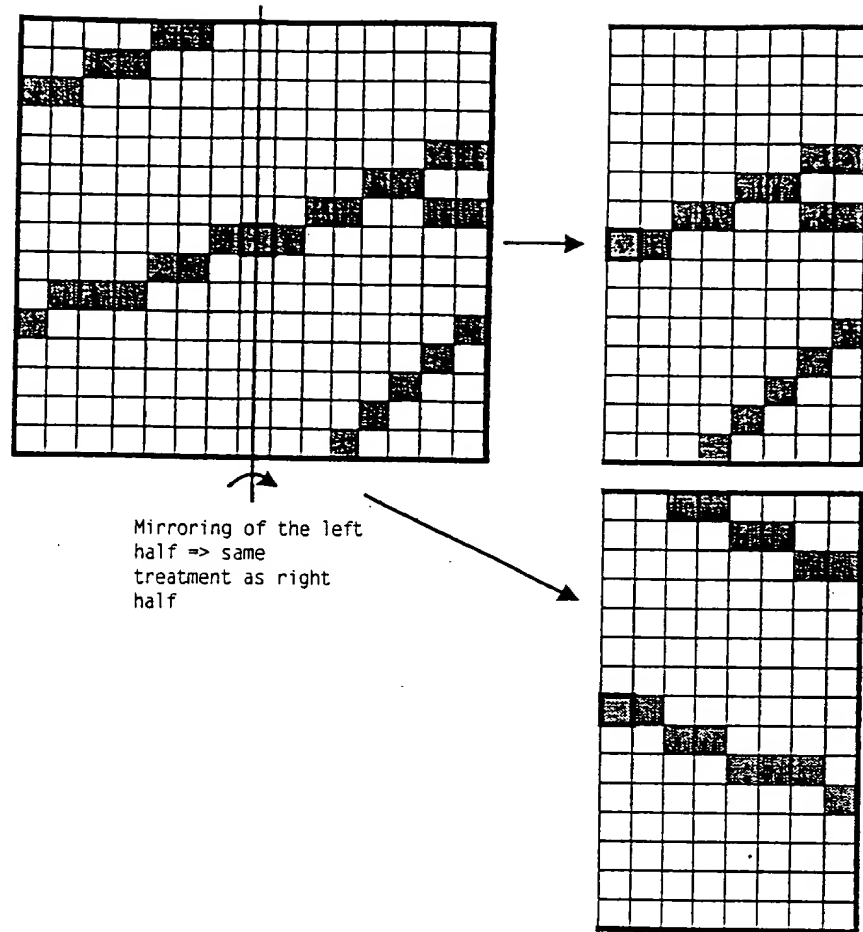


Fig. 15

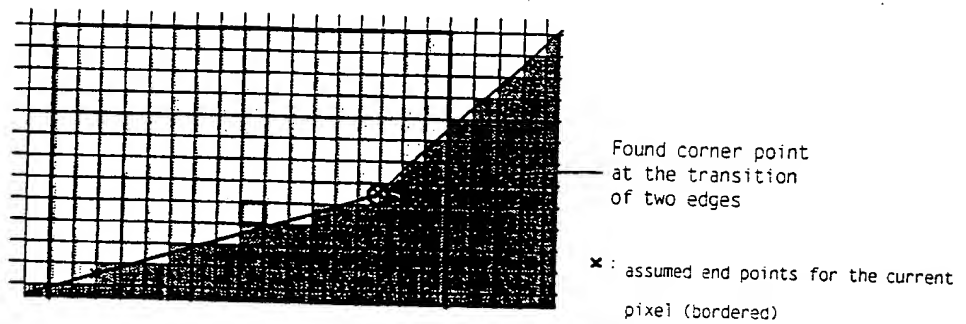


Fig. 17

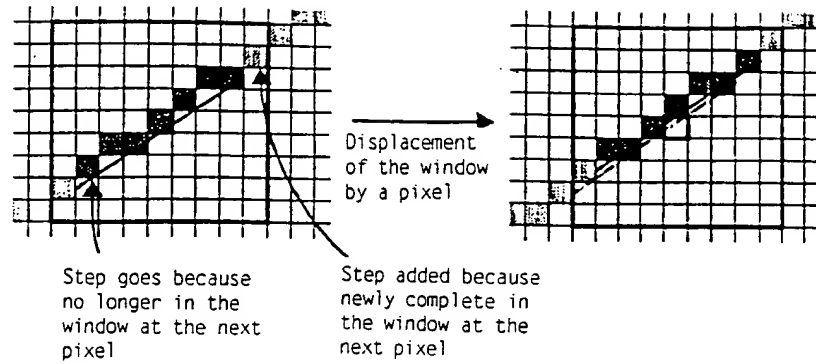


Fig. 18

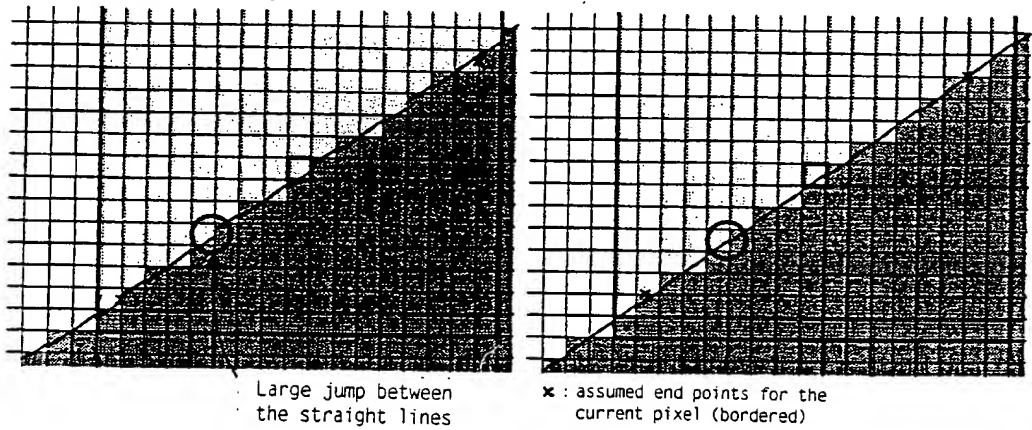


Fig. 19

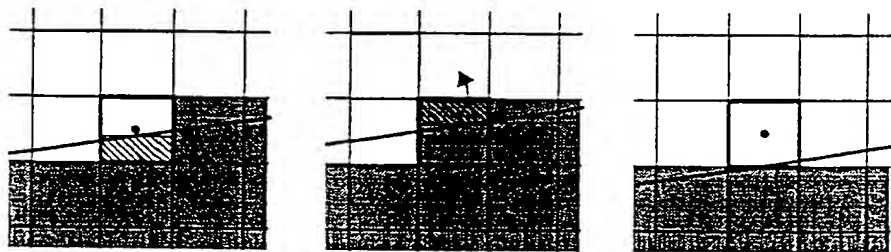


Fig. 20

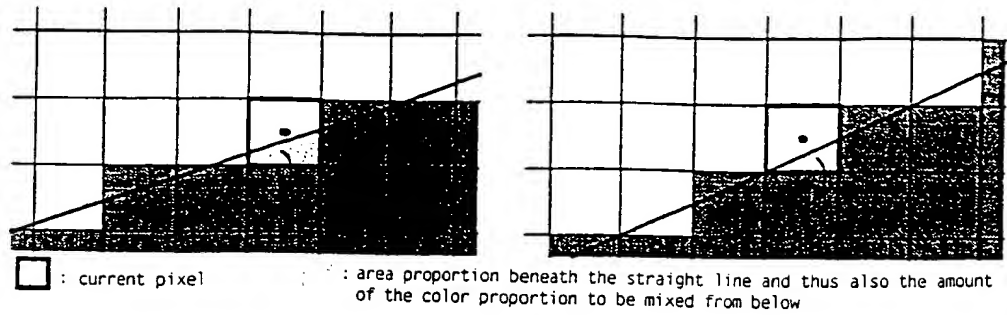


Fig. 21

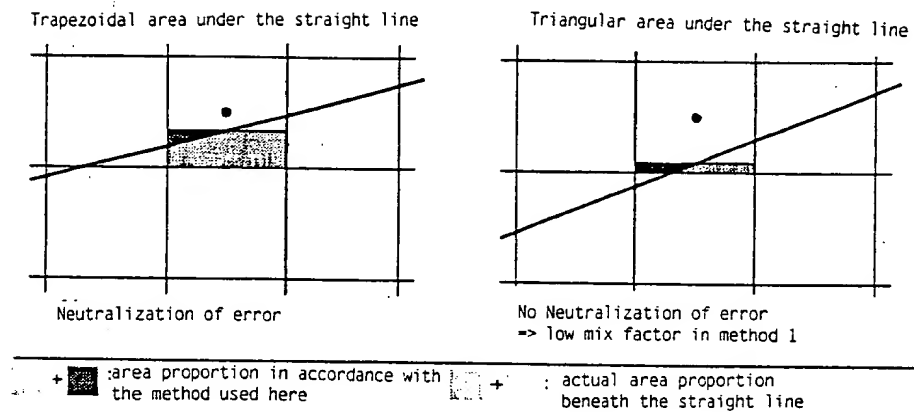


Fig. 22

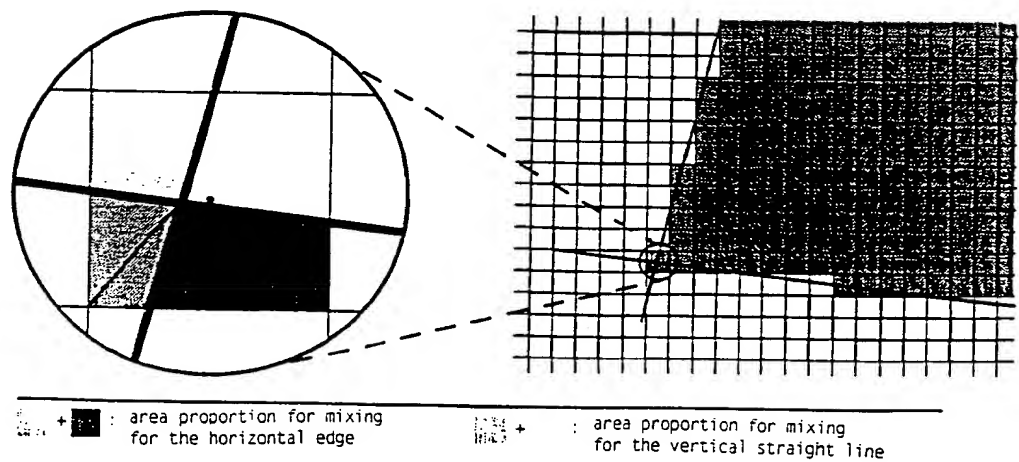


Fig. 23

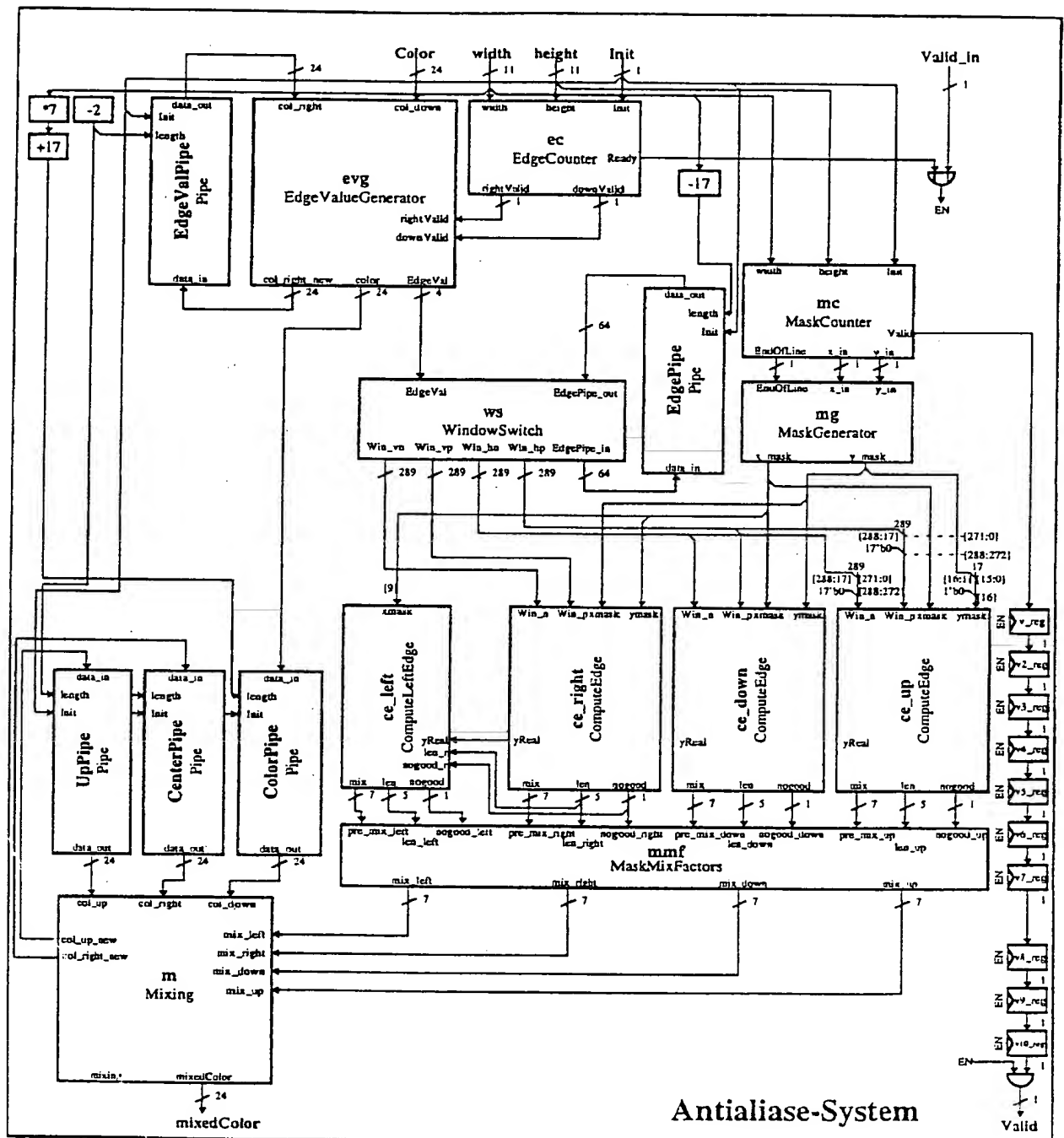


Fig. 24

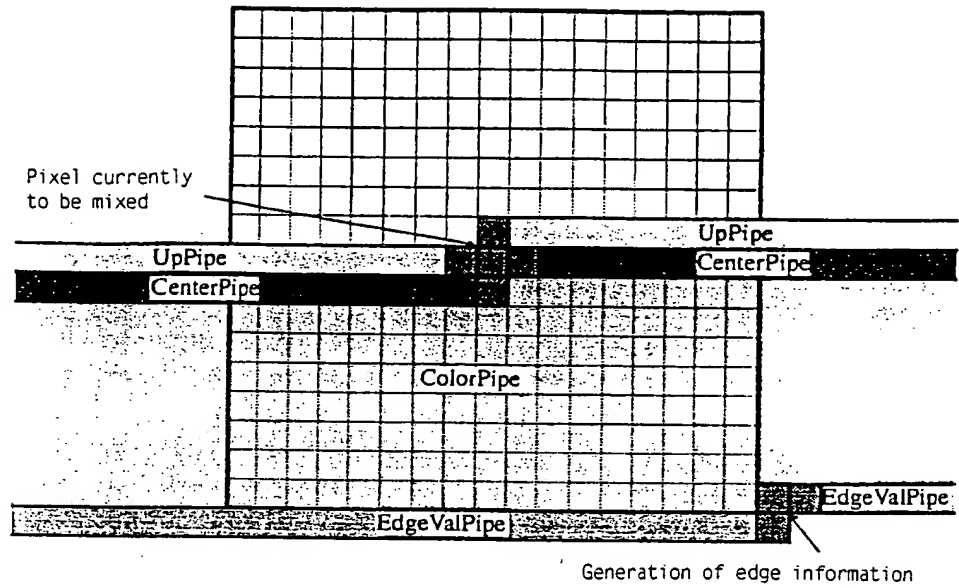


Fig. 25

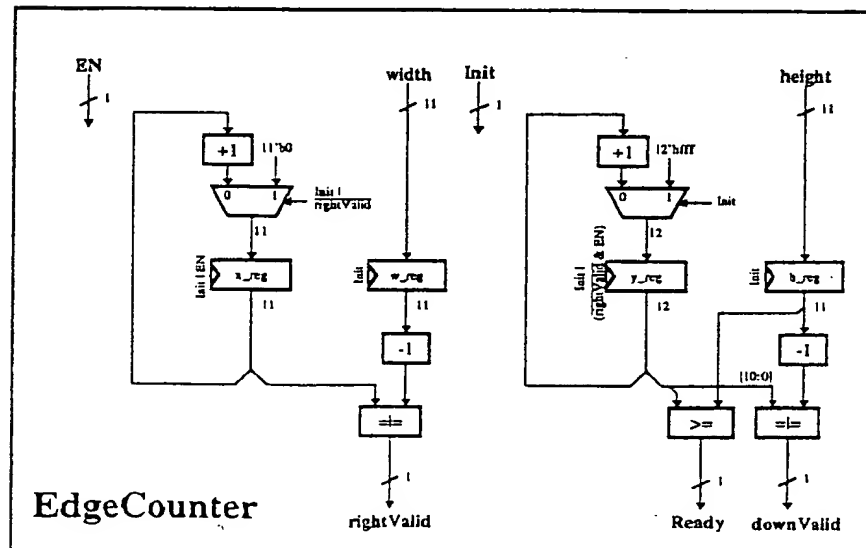


Fig. 26

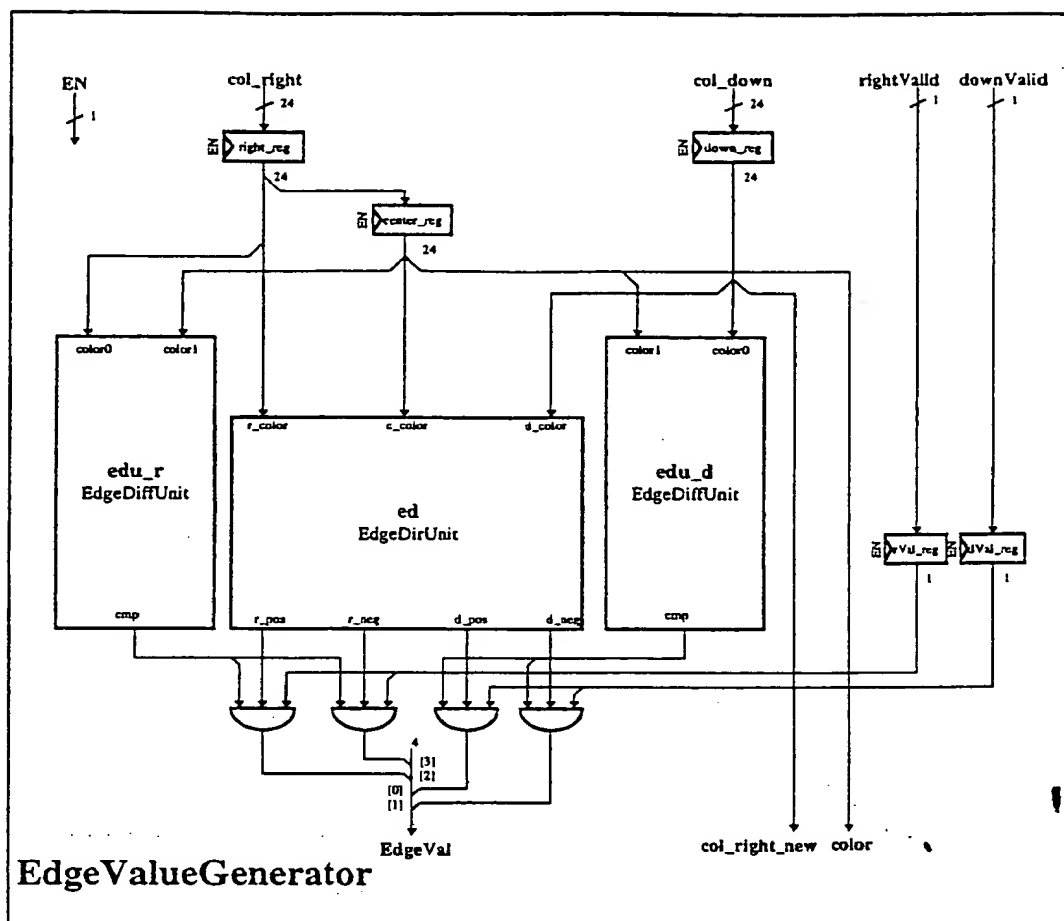


Fig. 27



Fig. 28



Fig. 29

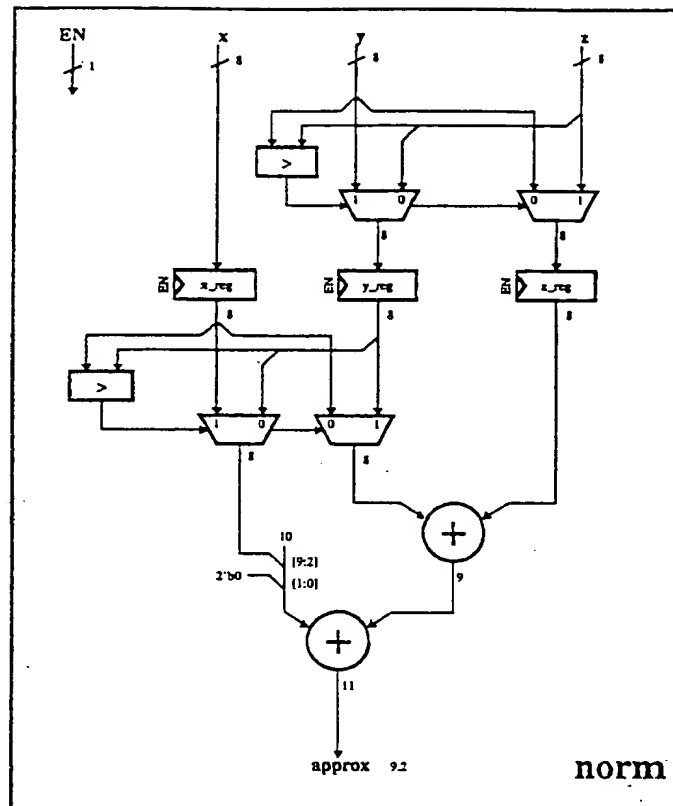


Fig. 30

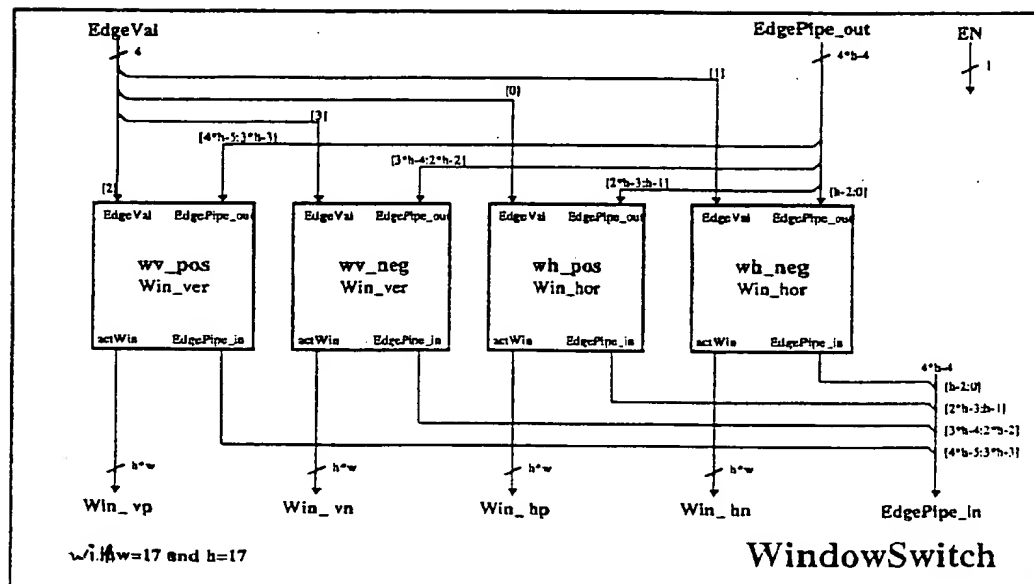


Fig. 31

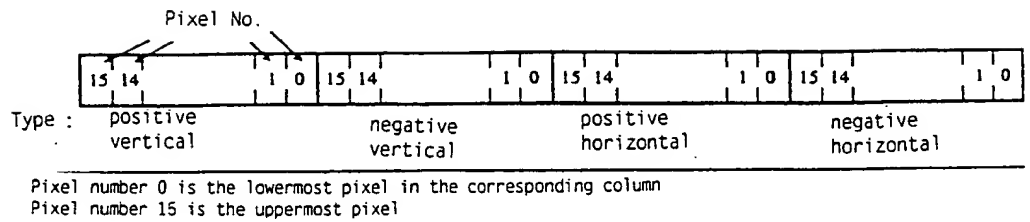


Fig. 32

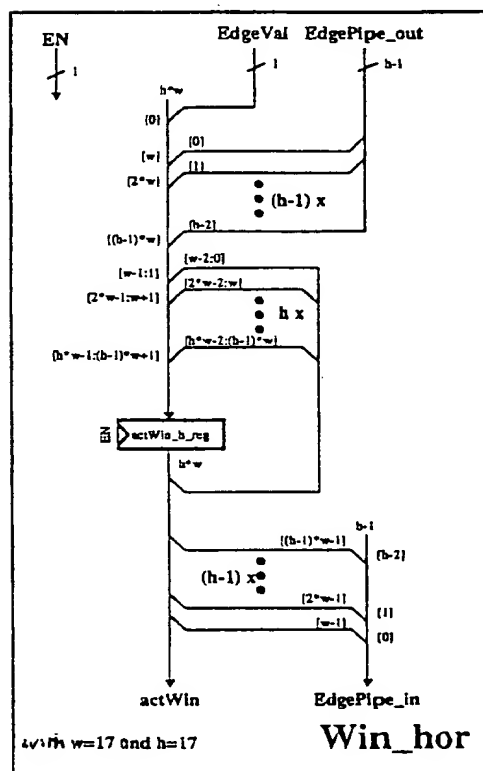


Fig. 33

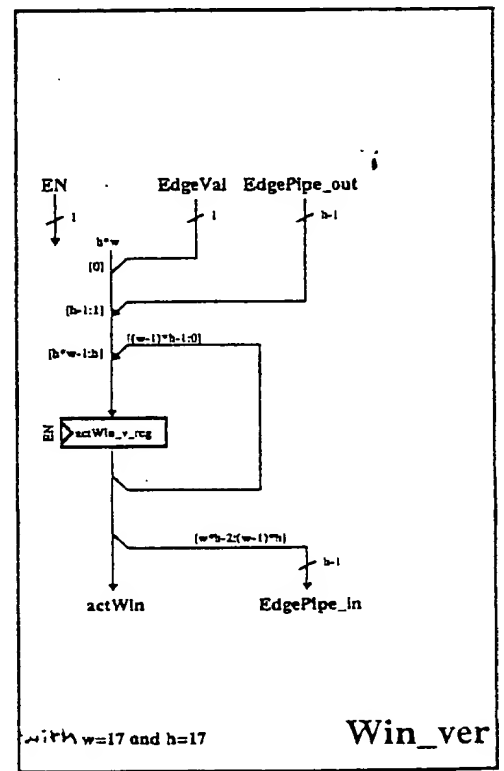


Fig. 34

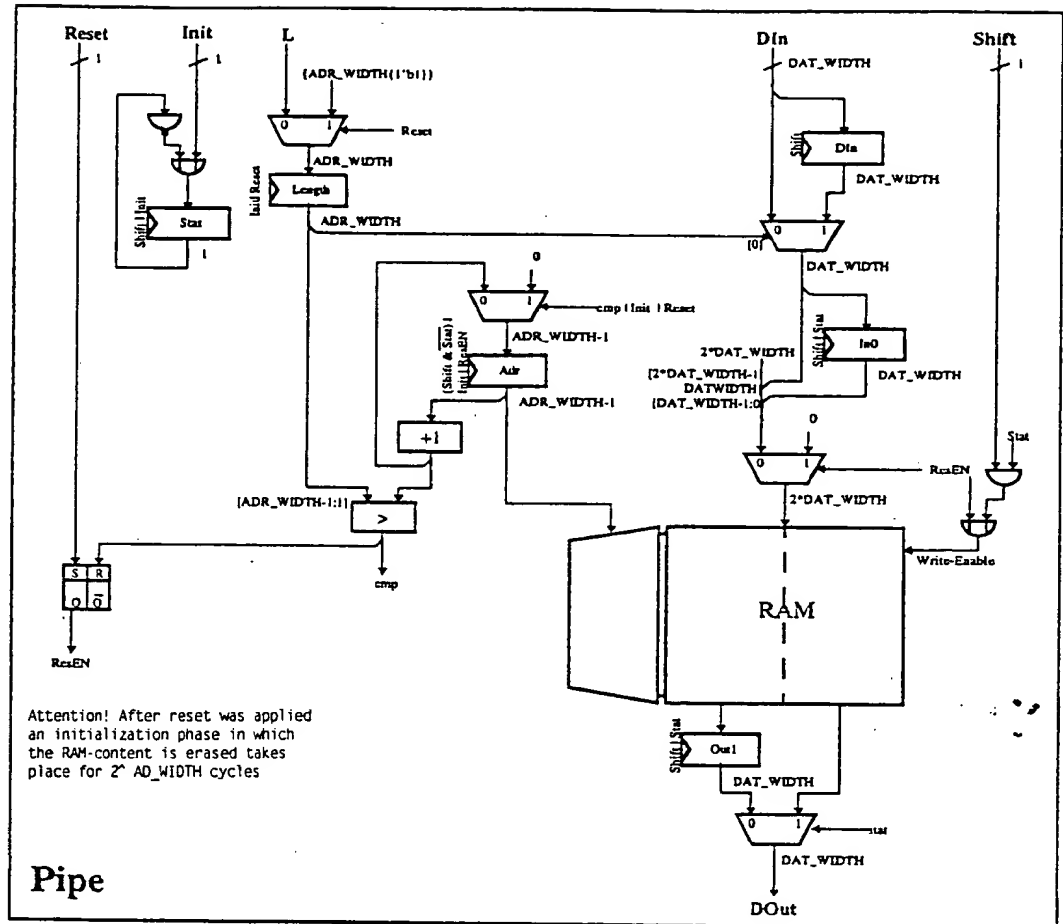


Fig. 35

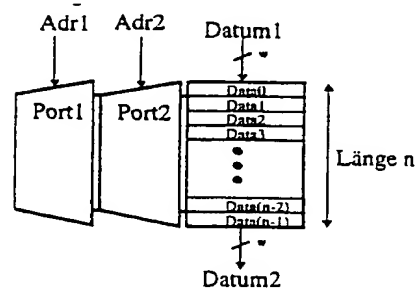


Fig. 36

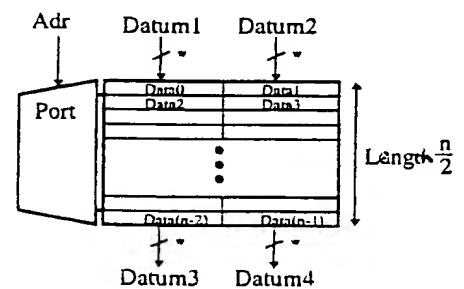


Fig. 37

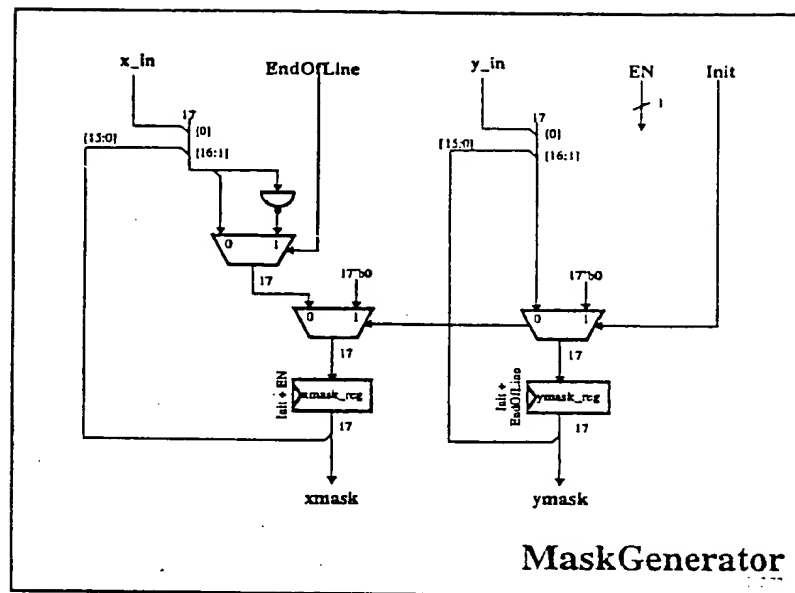


Fig. 38

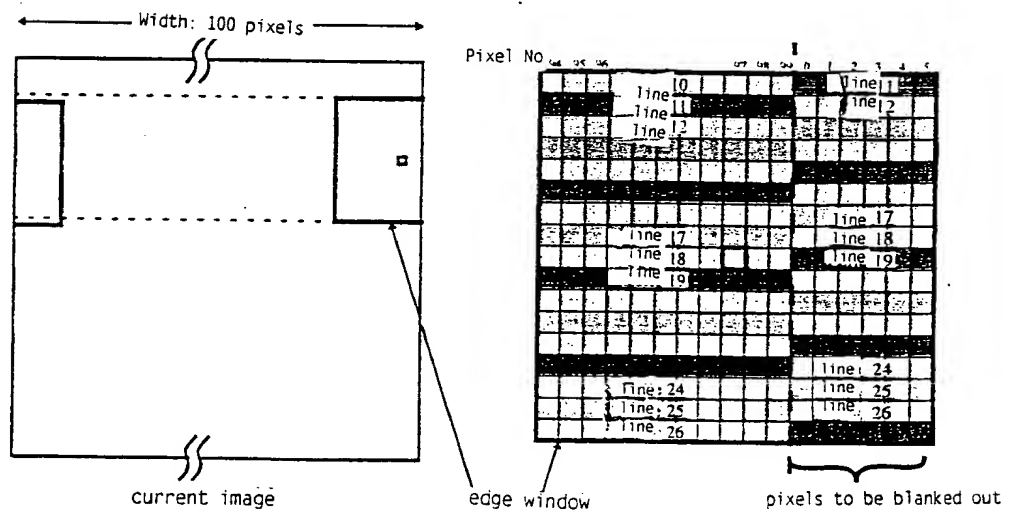


Fig. 39

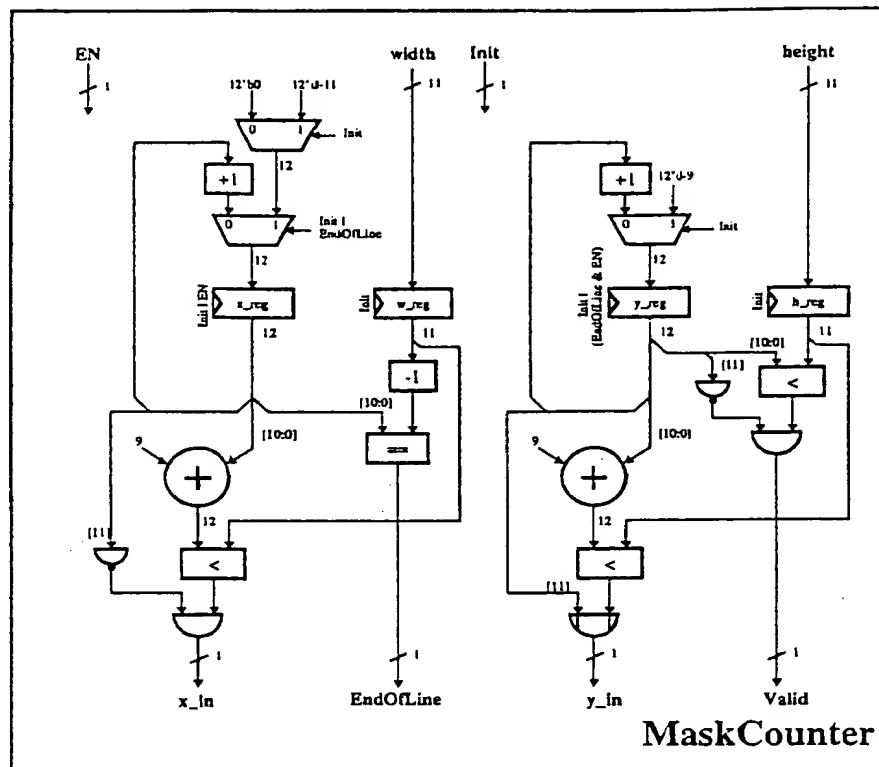


Fig. 40

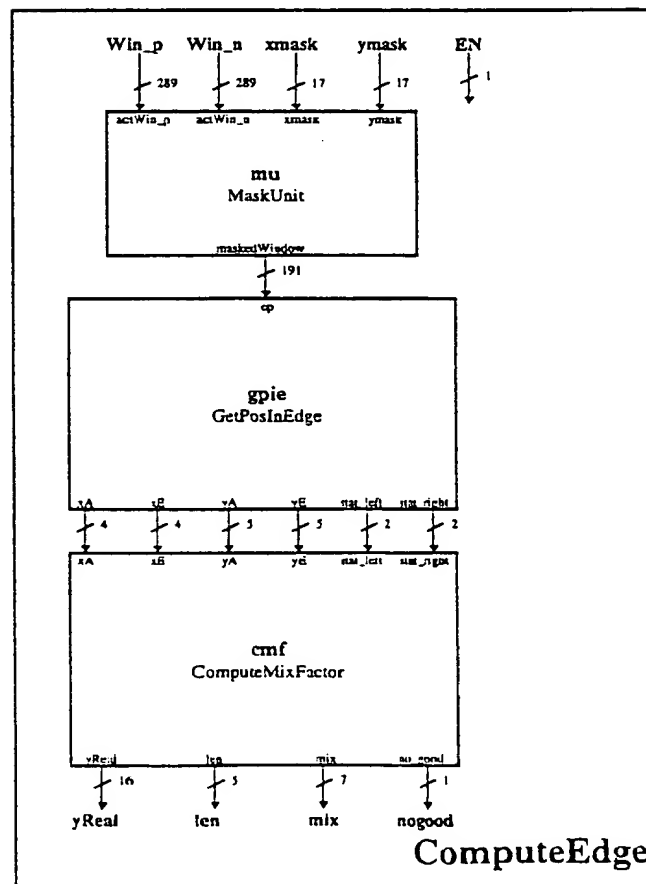


Fig. 41

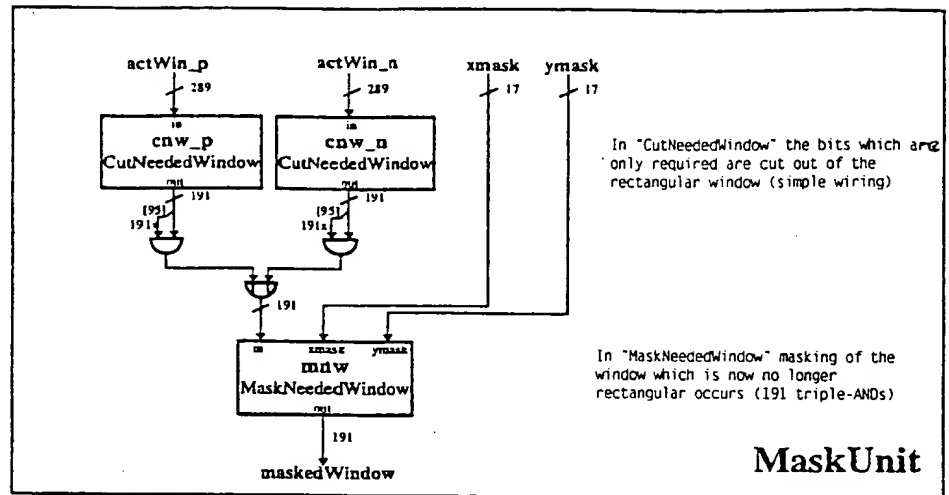


Fig. 42

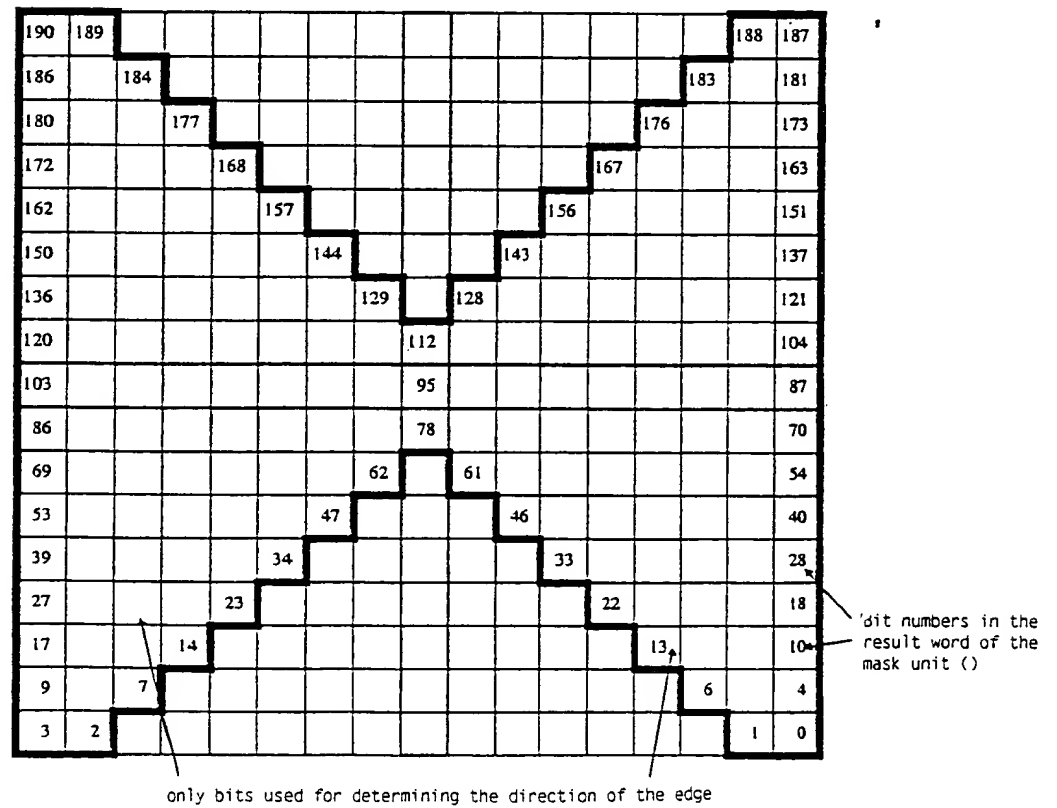


Fig. 43

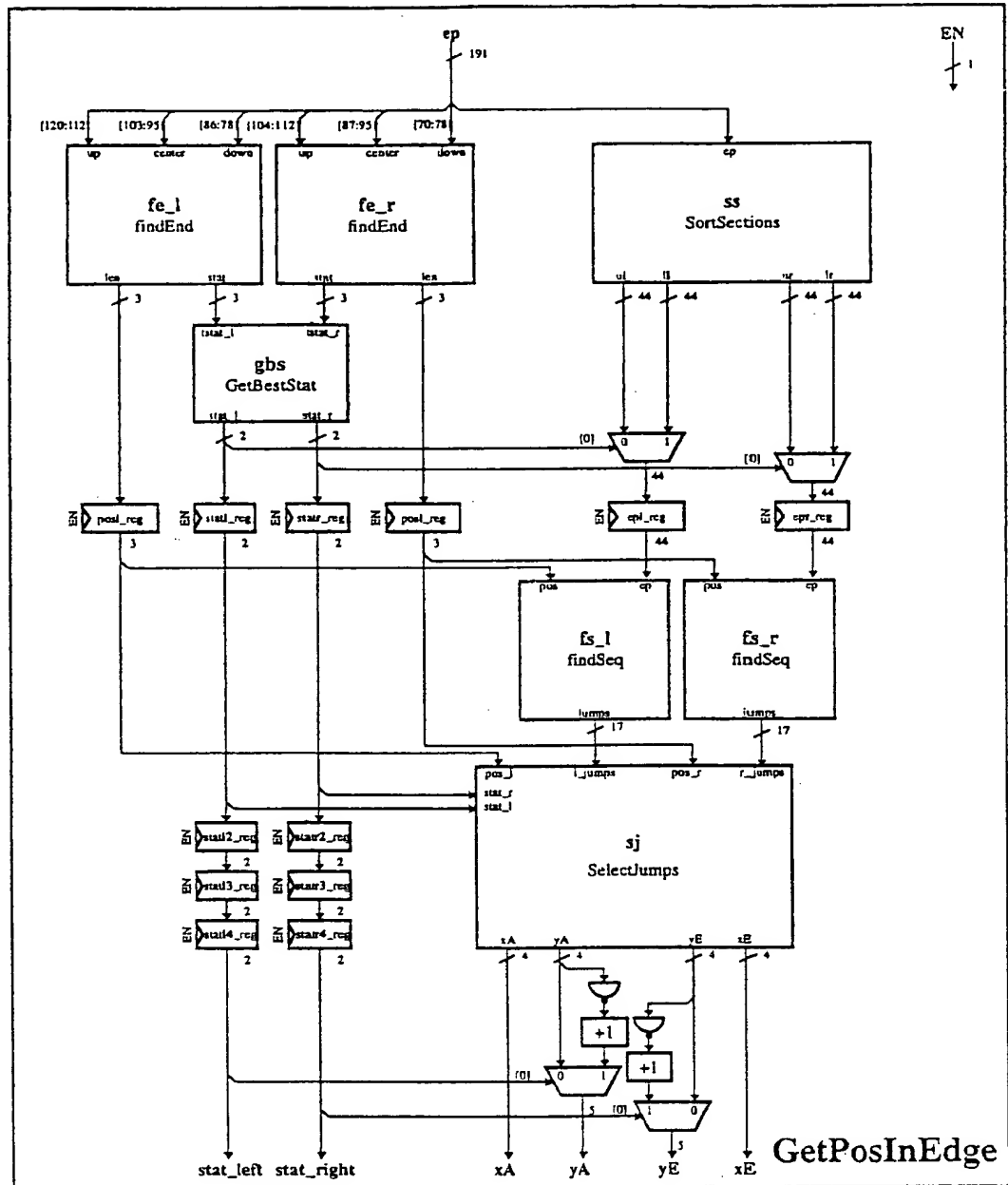


Fig. 44

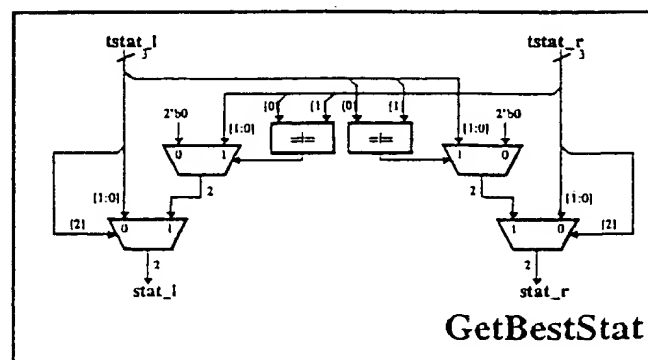


Fig. 45

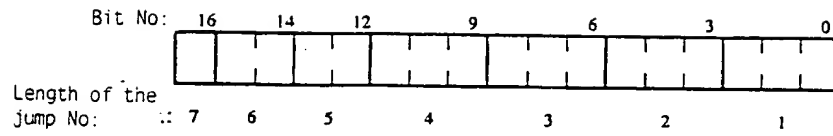


Fig. 46

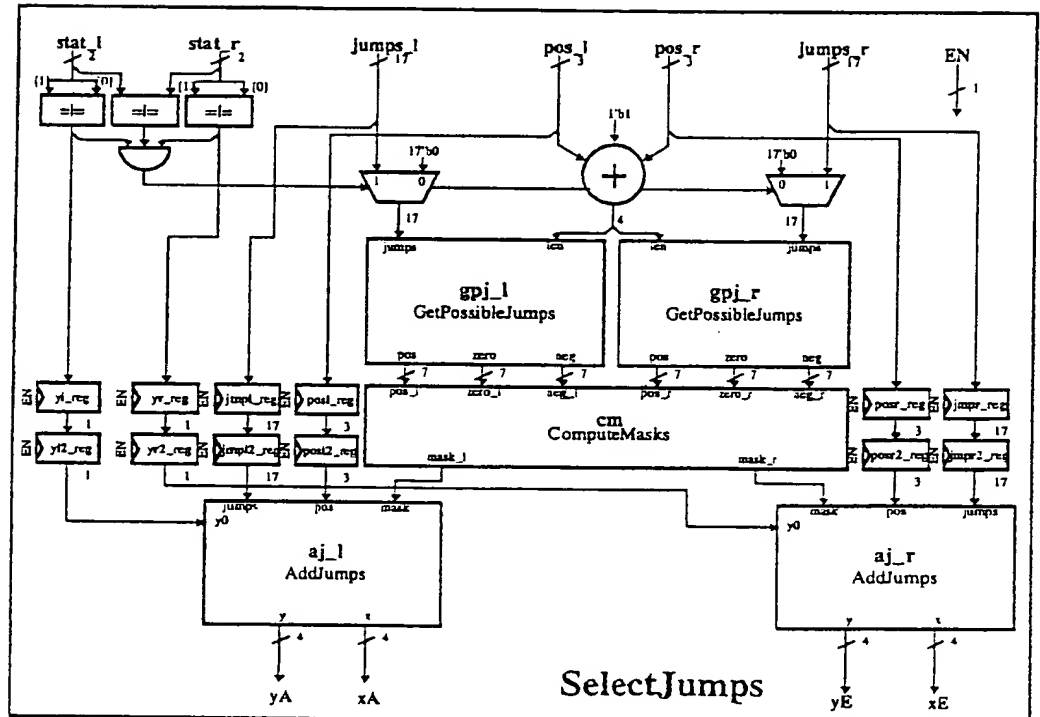


Fig. 47

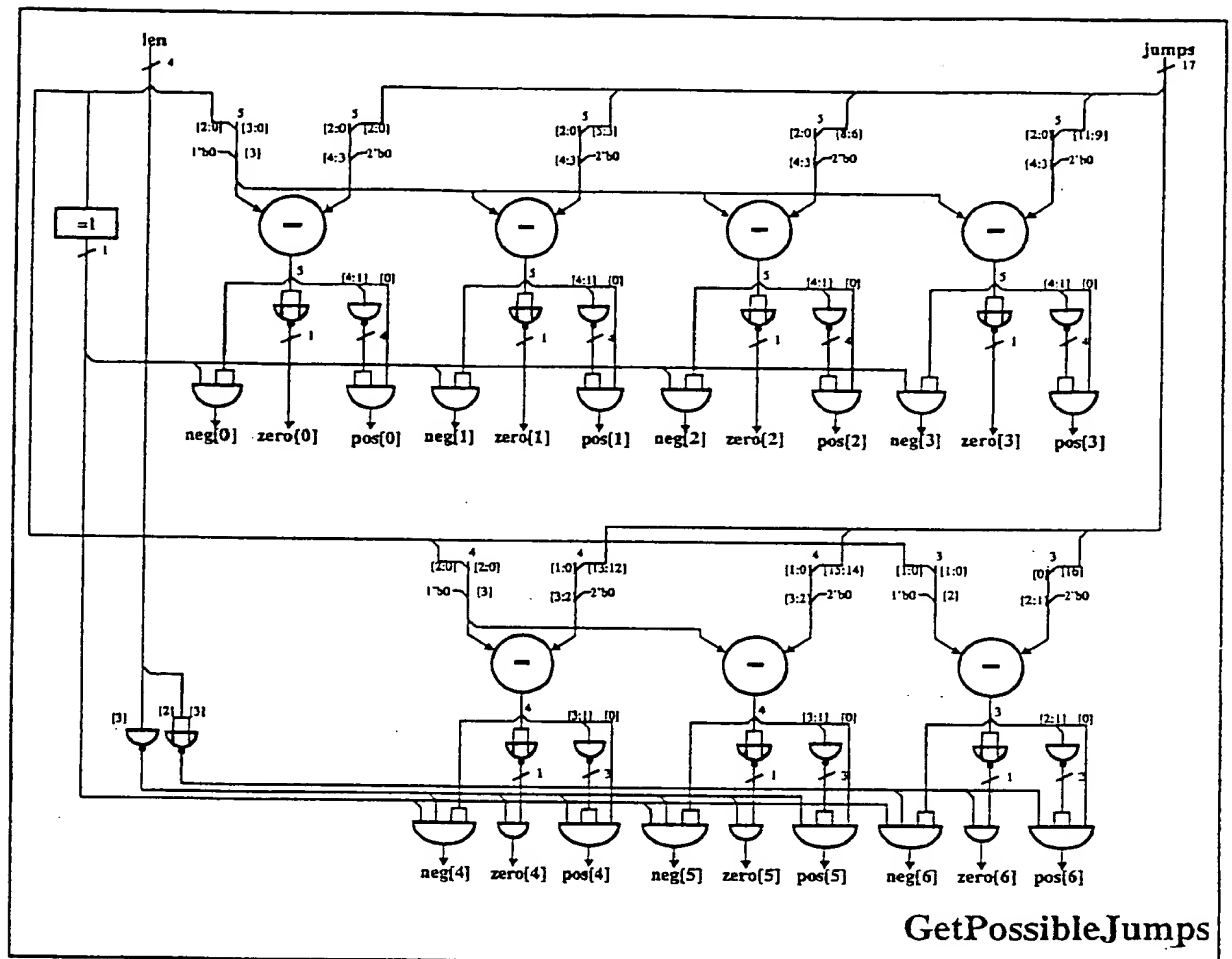


Fig. 48

Fig. 49

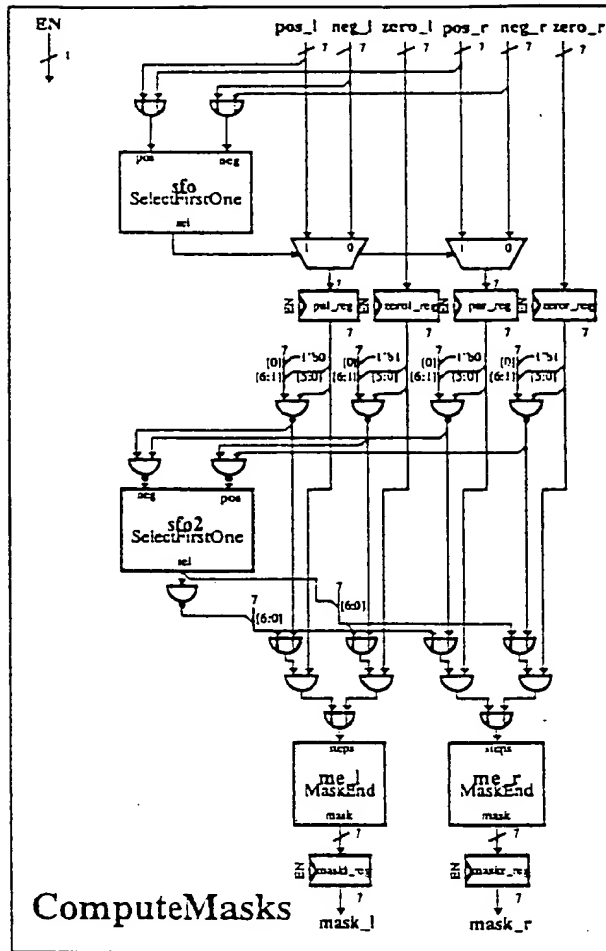
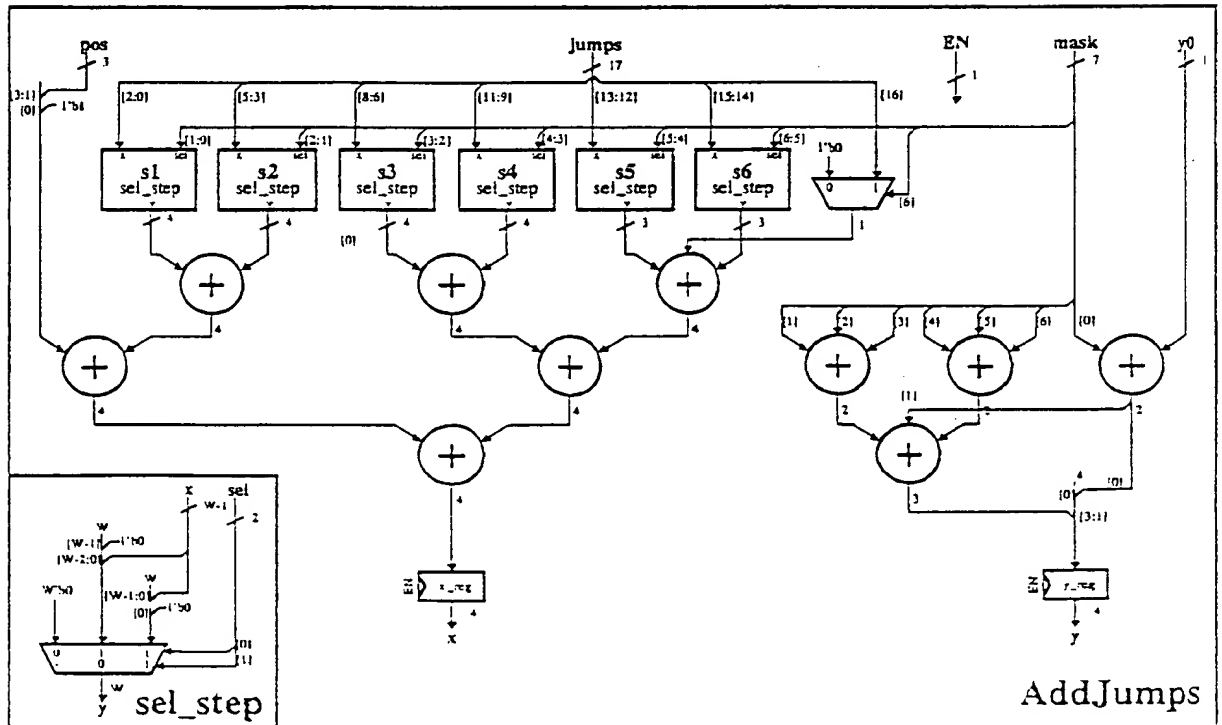


Fig. 50



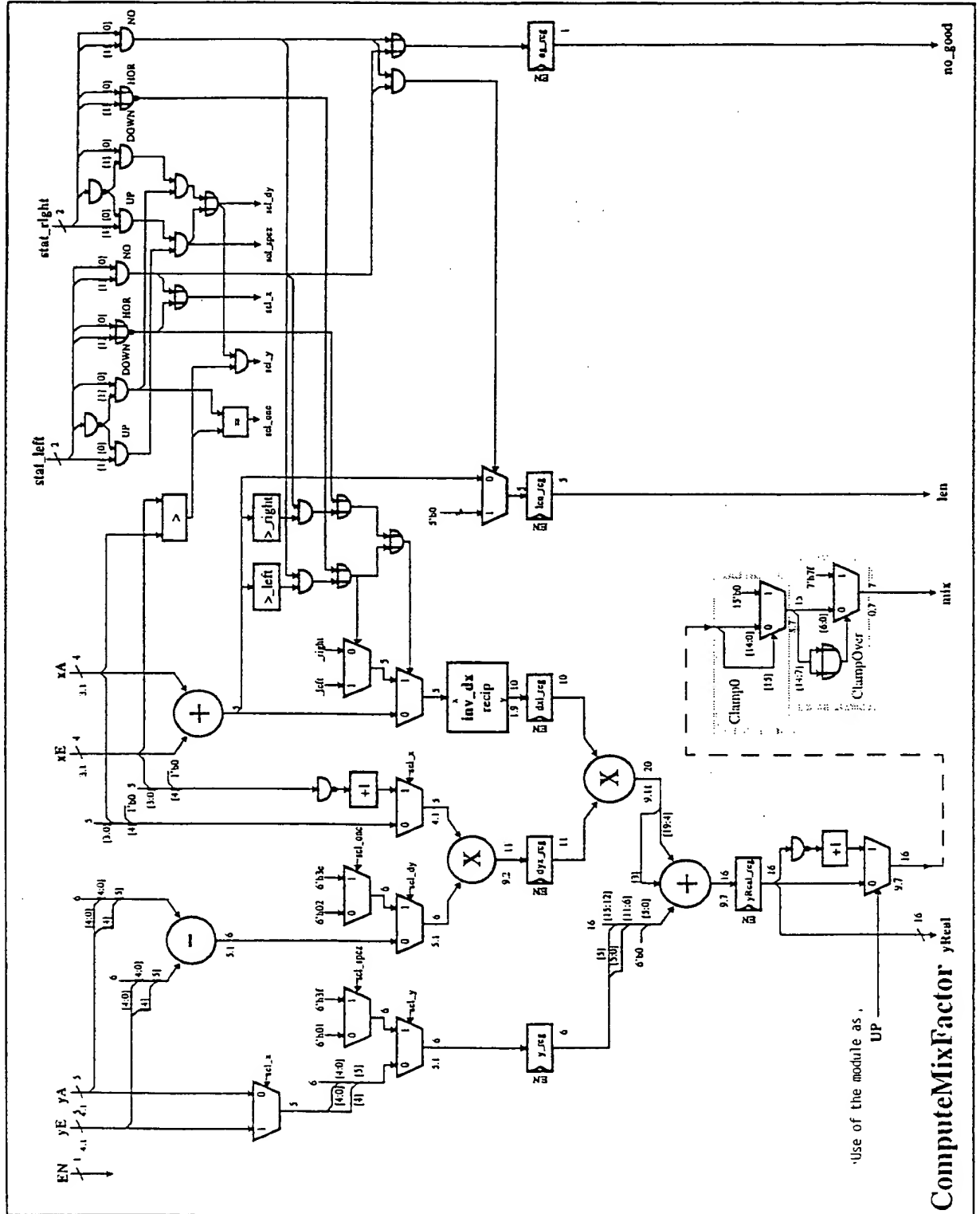


Fig. 51

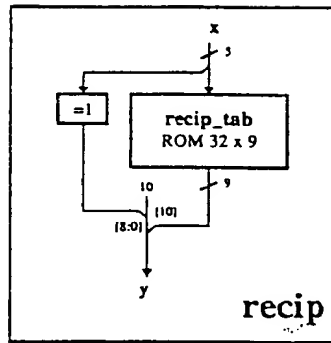


Fig. 52

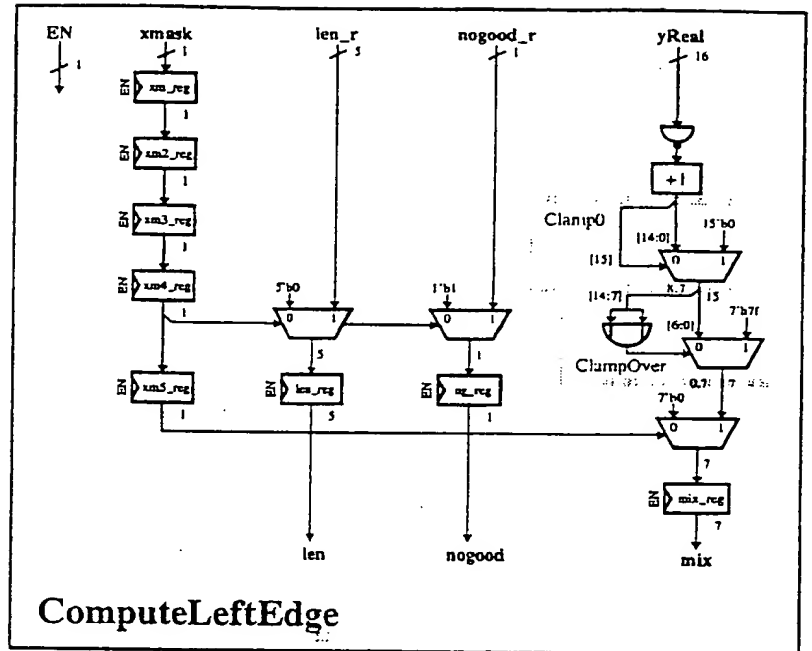


Fig. 53

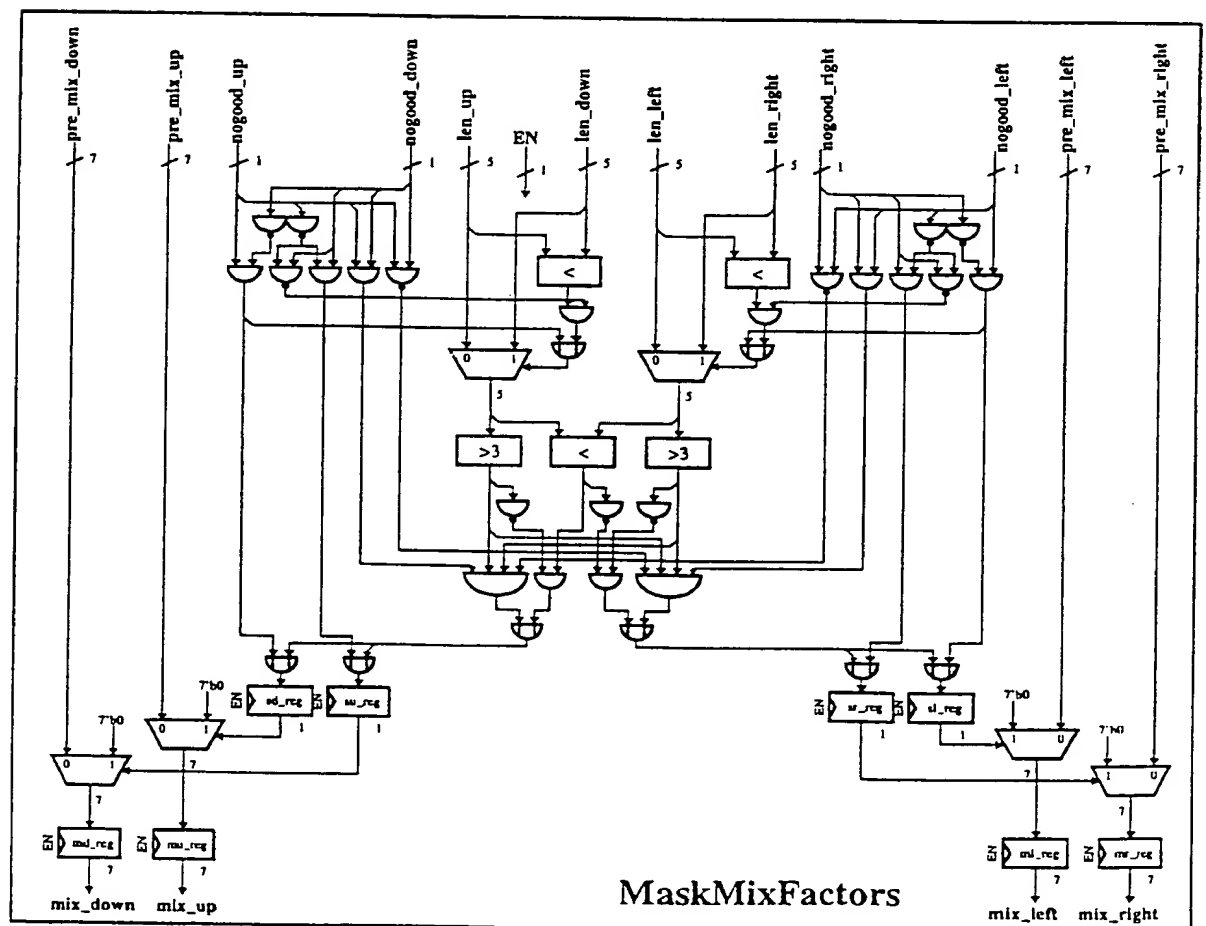


Fig. 54

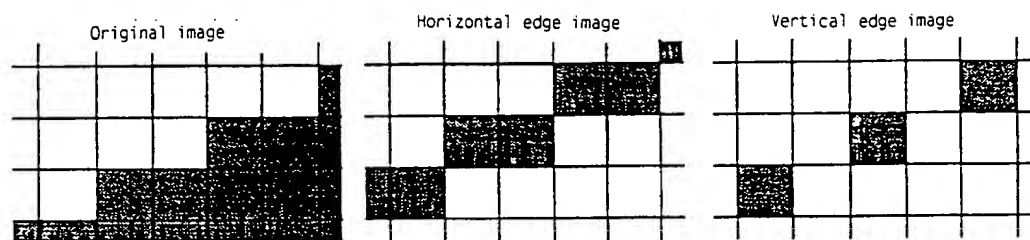


Fig. 55

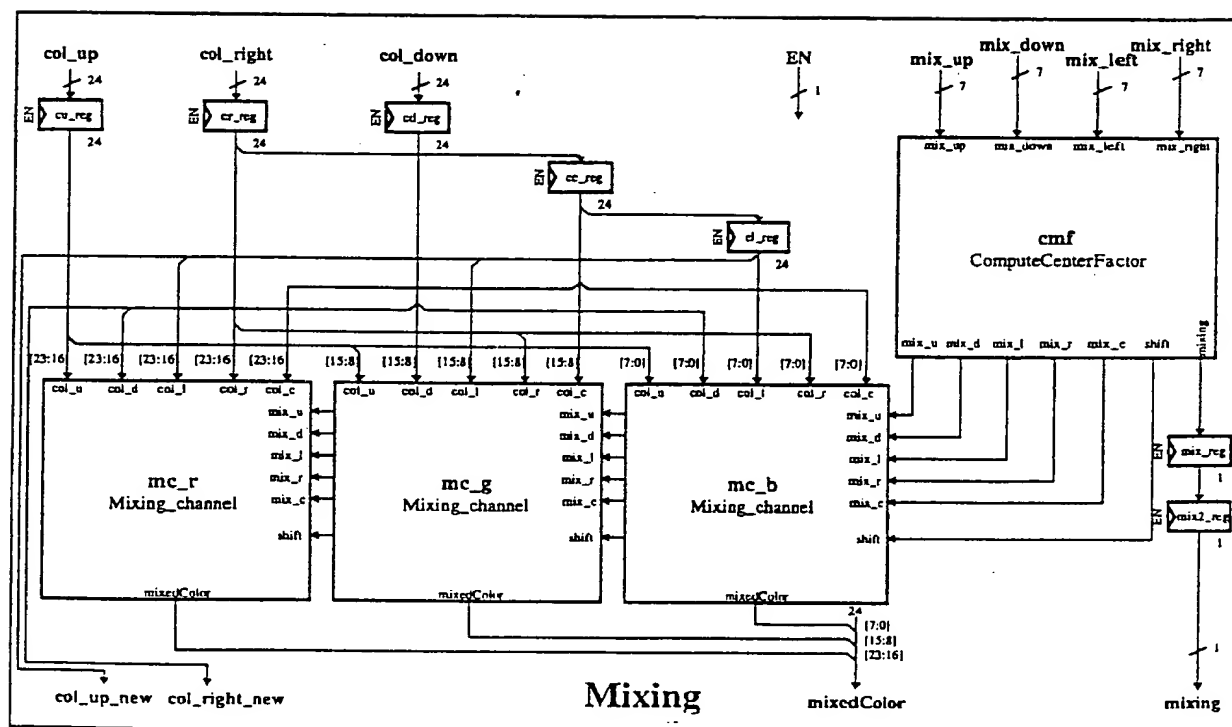


Fig. 56

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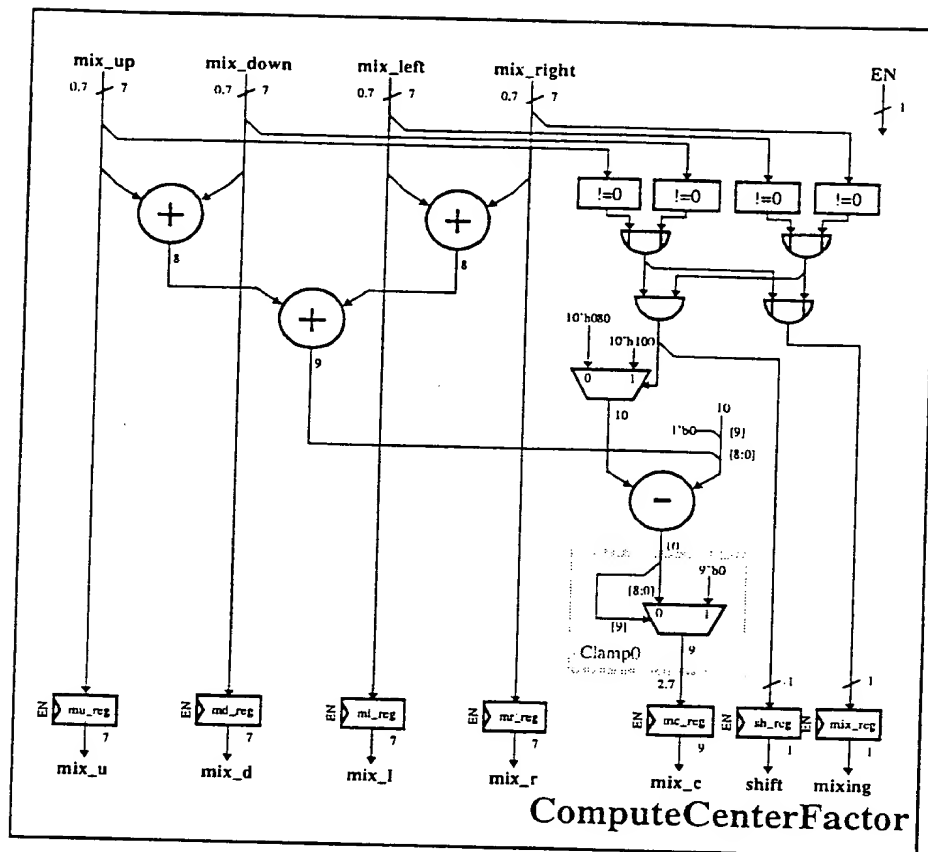


Fig. 57

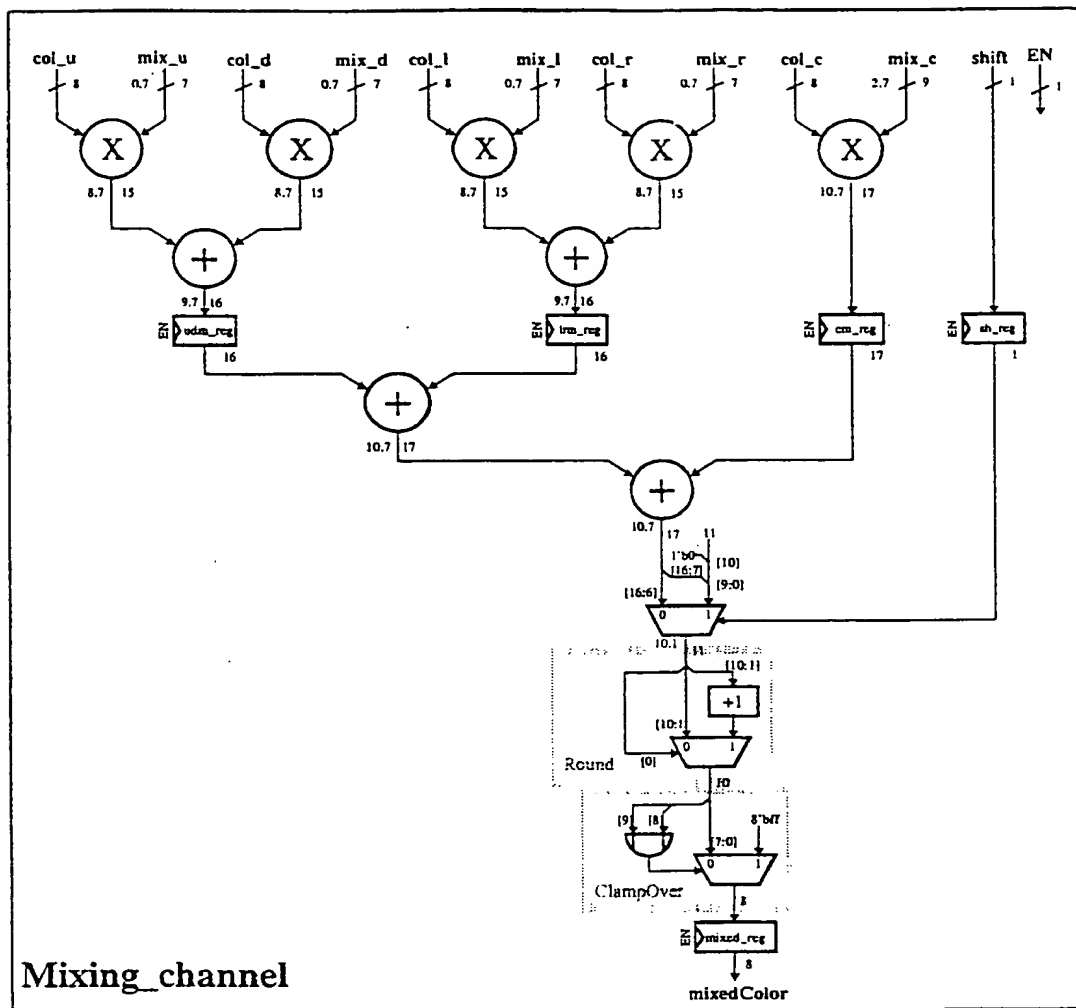


Fig. 58

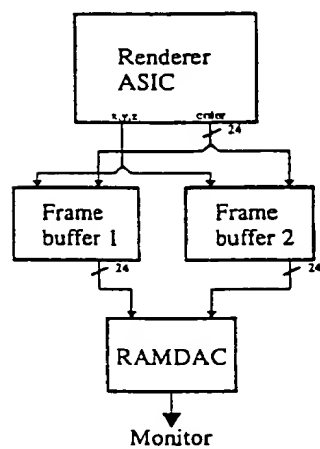


Fig. 59

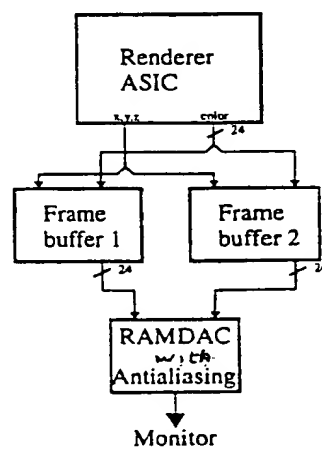


Fig. 60

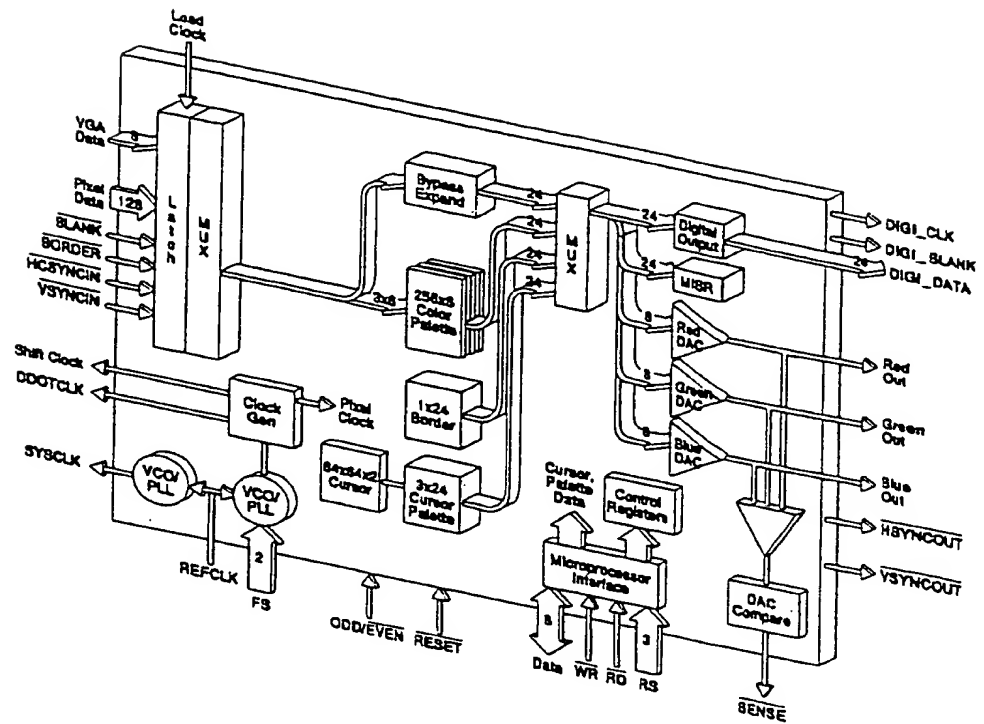


Fig. 61

Fig. 62

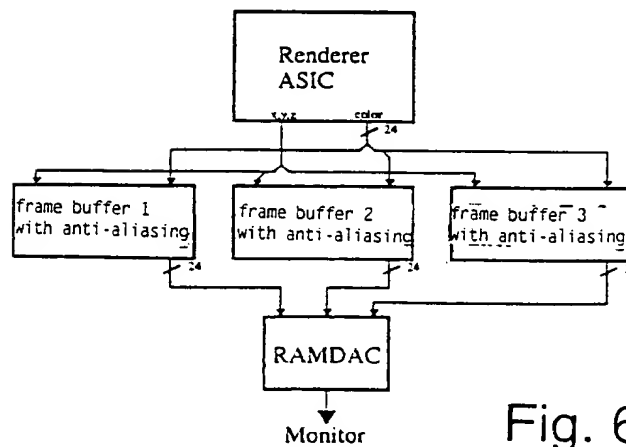
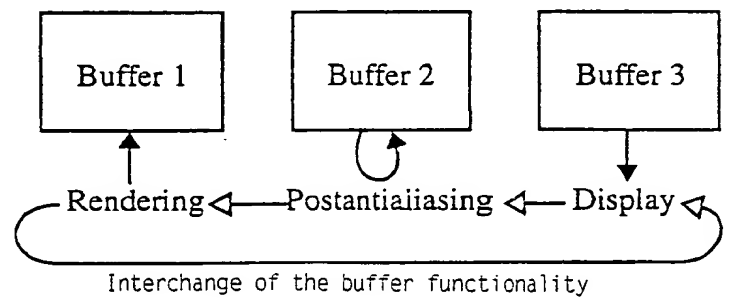


Fig. 63

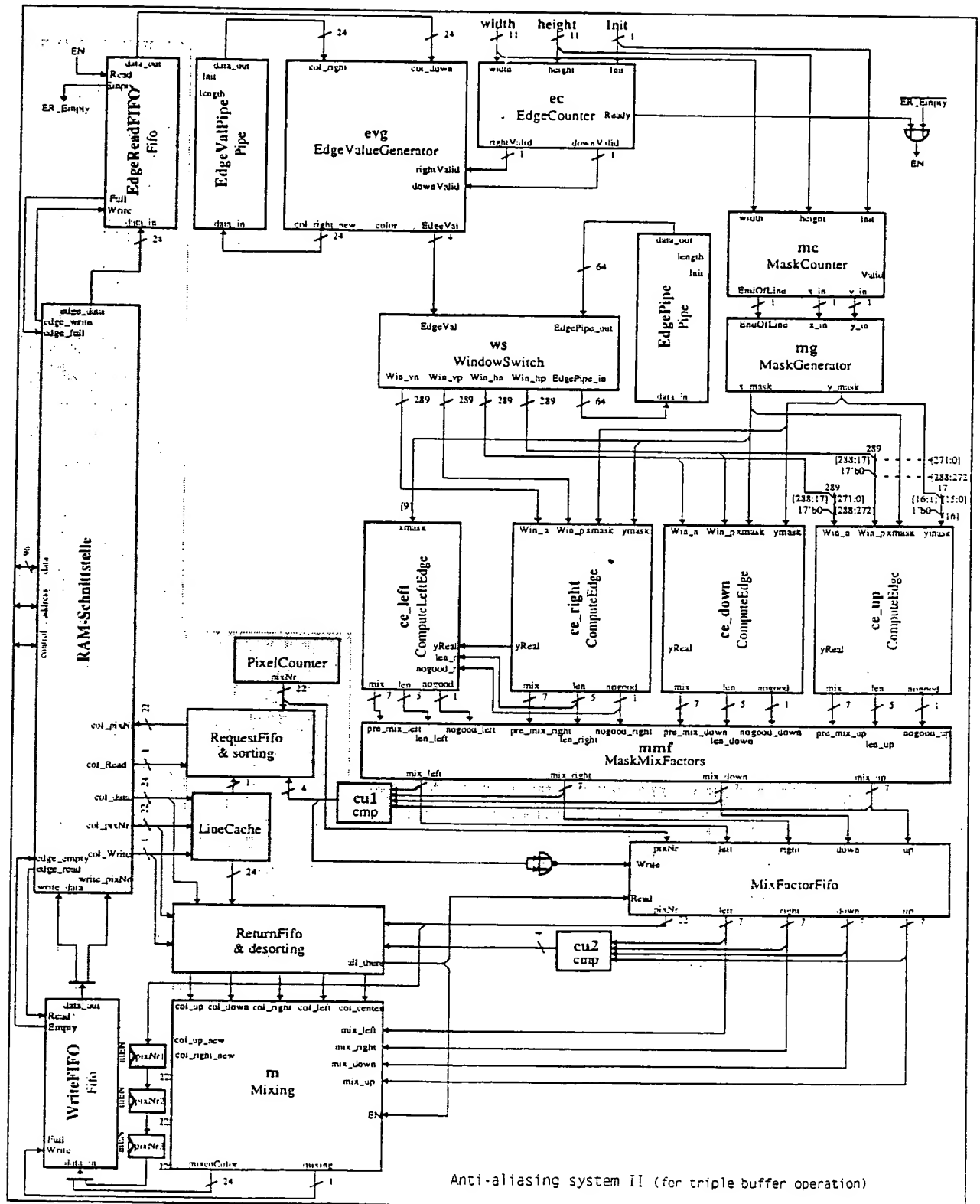


Fig. 64

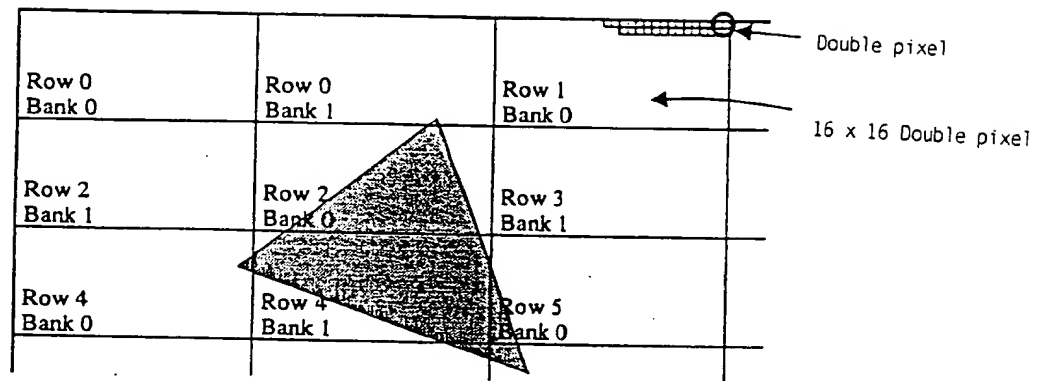


Fig. 65

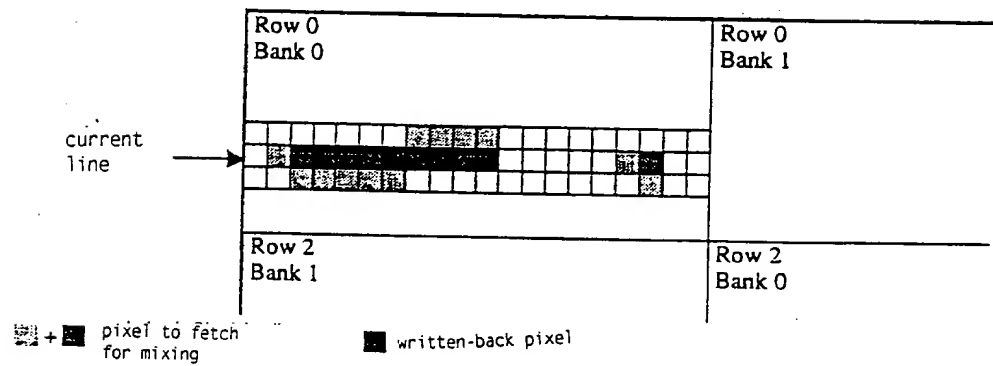
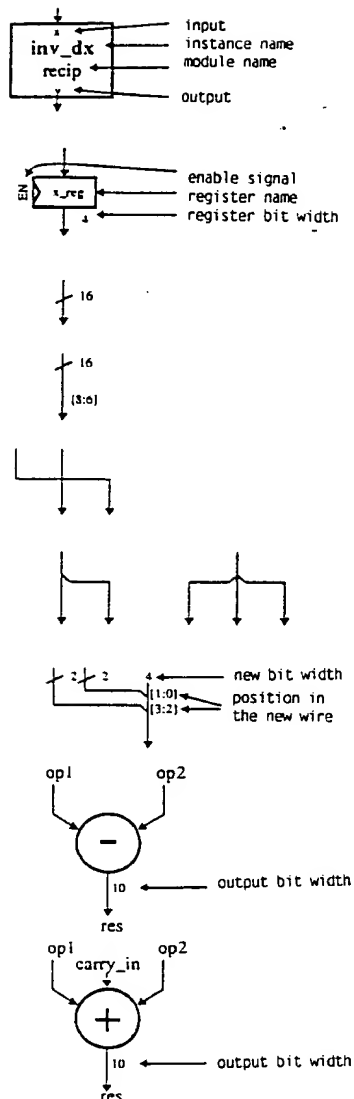


Fig. 66



instanting of a self-defined module

register: the datum at the input is transferred at the positive clock edge if the enable signal is set

Bit width of a wire

Selection of bits of a wire

Mutually crossing wires without galvanic connection

Branching of a wire

Concatenation of bits

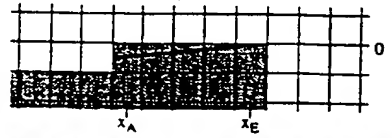
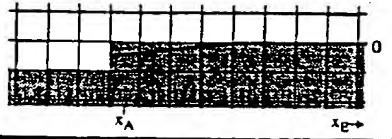
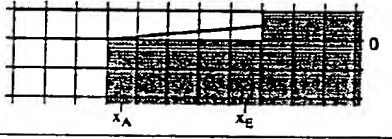
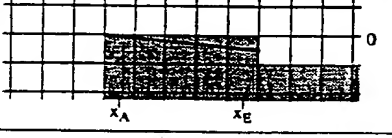
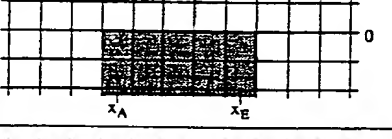
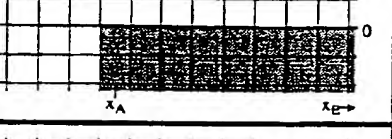
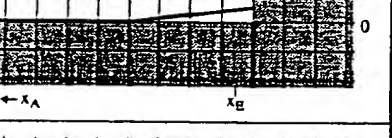
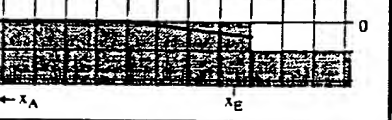
Subtraction ($res = op1 - op2$ and not the other way round)

Addition (the middle input is only a carry input and thus only 1 bit wide, as cost this element counts as an addition of two number ...)

Fig. 67

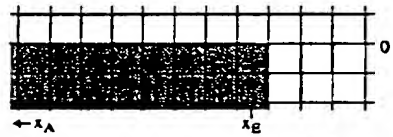
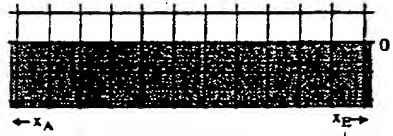
Start status	End status	Straight line through the points	Example
UP	UP	$(x_A - 0.5, 0.5) - (0.5 \cdot (x_A + x_E), 0)$ for $x \leq 0.5 \cdot (x_A + x_E)$ $(0.5 \cdot (x_A + x_E), 0) - (x_E + 0.5, 0.5)$ for $x > 0.5 \cdot (x_A + x_E)$	
UP	DOWN	$(x_A - 0.5, 0.5) - (x_E + 0.5, -0.5)$	
UP	NO	$(x_A - 0.5, 0.5) - (x_E + 0.5, 0)$	
UP	HOR	$(x_A - 0.5, 0.5) - (x_A + 0.5 \cdot (n-2), 0)$	
DOWN	UP	$(x_A - 0.5, -0.5) - (x_E + 0.5, 0.5)$	
DOWN	DOWN	$(x_A - 0.5, -0.5) - (0.5 \cdot (x_A + x_E), 0)$ for $x \leq 0.5 \cdot (x_A + x_E)$ $(0.5 \cdot (x_A + x_E), 0) - (x_E + 0.5, -0.5)$ for $x > 0.5 \cdot (x_A + x_E)$	

Tab. 1

Start status	End status	Straight line through the points	Example
DOWN	NO	$(x_A - 0.5, -0.5) - (x_E + 0.5, 0)$	
DOWN	HOR	$(x_A - 0.5, -0.5) - (x_A + 0.5 * (n-2), 0)$	
NO	UP	$(x_A - 0.5, 0) - (x_E + 0.5, 0.5)$	
NO	DOWN	$(x_A - 0.5, 0) - (x_E + 0.5, -0.5)$	
NO	NO	$y \equiv 0$	
NO	HOR	$y \equiv 0$	
HOR	UP	$(x_E - 0.5 * (n-2), 0) - (x_E + 0.5, 0.5)$	
HOR	DOWN	$(x_E - 0.5 * (n-2), 0) - (x_E + 0.5, -0.5)$	

Tab. 2

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Start status	End status	Straight line through the points	Example
HOR	NO	$y \equiv 0$	
HOR	HOR	$y \equiv 0$	

Tab. 3

Signal	Bits	Type	Description
Init	1	In	Initialization signal (transfer of a new height and width)
width	11	In	New display screen width (only relevant at Init=1)
height	11	In	New display screen height (only relevant at Init=1)
Color	24	In	Chromaticity value of a pixel
Valid_in	1	In	Validity display of the color signal
mixedColor	24	Out	Anti-aliased chromaticity value of a pixel
Valid	1	Out	Validity display of the mixed color signal

Tab. 4

Signal	Bits	Type	Description
EN	1	In	Enable signal of the counters
Init	1	In	Initialization signal (transfer of the new width and height)
width	11	In	New display screen width (only relevant at Init=1)
height	11	In	New display screen height (only relevant at Init=1)
rightValid	1	Out	Validity display of the pixel right of the current one
downValid	1	Out	Validity display of the pixel below the current one
Ready	1	Out	Display that all pixels of the current image were read in

Tab. 5

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
col_right	24	In	Chromaticity value for the pixel right of the current one
col_down	24	In	Chromaticity value for the pixel below the current one
rightValid	1	In	Validity display of the col_right signal
downValid	1	In	Validity display of the col_down signal
EdgeVal	4	Out	Edge information for the current pixel
col_right_new	24	Out	Chromaticity value which is used again for edge generation in the next line
color	24	Out	Chromaticity value which is to be stored for later mixing

Tab. 6

Signal	Bits	Type	Description
EN	1	In	Enable signal of the module
color0	24	In	Color of the one pixel
color1	24	In	Color of the other pixel between which an edge is to be recognised
cmp	1	Out	Indication whether an edge exists between the pixels involved

Tab. 7

Signal	Bits	Type	Description
EN	1	In	Enable signal of the module
r_color	24	In	Color of the right pixel
c_color	24	In	Color of the central pixel
d_color	24	In	Color of the lower pixel
r_pos	1	Out	There is a positive color jump from the central to the right pixel
r_neg	1	Out	There is a negative color jump from the central to the right pixel
d_pos	1	Out	There is a positive color jump from the central to the lower pixel
d_neg	1	Out	There is a negative color jump from the central to the lower pixel

Tab. 8

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
x	8	In	Chromaticity value of a channel
y	8	In	Chromaticity value of a channel
z	8	In	Chromaticity value of a channel
approx	11	Out	Result value

Tab. 9

Signal	Bits	Type	Description
EN	1	In	Enable signal of the module
EdgeVal	4	In	New edge value for the right lower pixel in the edge window
EdgePipe_out	64	In	Edge values of the most right column
Win_vp	289	Out	Edge window with the vertically positively marked pixels
Win_vn	289	Out	Edge window with the vertically negatively marked pixels
Win_hp	289	Out	Edge window with the horizontally positively marked pixels
Win_hn	289	Out	Edge window with the horizontally negatively marked pixels
EdgePipe_in	64	Out	Edge values of the column most to the left, which are no longer required for the current window (relevant again only when processing the next line)

Tab. 10

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
EdgeVal	1	In	New edge value for the right lowermost pixel
EdgePipe_out	16	In	Edge value for the most right column
actWin	289	Out	Vertical/horizontal edge window
EdgePipe_in	16	Out	Edge values of the column most to the left, which are no longer required for the current window (relevant again only when processing the next line)

Tab. 11

Signal	Bits	Type	Description
Reset	1	In	Reset signal, after application of this signal an RAM initialization phase occurs
Init	1	In	Initialization signal at which the length of the pipe is established again
L	?	In	New length of the pipe used (bit width can be established by way of parameters)
Shift	1	In	Signal for advancing the data (new datum is taken over, a datum is outputted)
DIn	?	In	Data input of the pipe (bit width can be established by way of parameters)
DOut	?	Out	Data output of the pipe (bit width can be established by way of parameters)

Tab. 12

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
Init	1	In	Initialization signals for the masks
x_in	1	In	New value for the x-mask
y_in	1	In	New value for the y-mask
EndOfLine	1	In	Signal which displays that the end of an image line is reached
xmask	17	Out	Mask which horizontally specifies which pixels belong to the current environment
ymask	17	Out	Mask which vertically specifies which pixels belong to the current environment

Tab. 13

Signal	Bits	Type	Description
EN	1	In	Enable signal of the counters
Init	1	In	Initialization signal (transfer of the new width and height)
width	11	In	New width (only relevant at Init=1)
height	11	In	New height (only relevant at Init=1)
EndOfLine	1	Out	Signal which indicates that the end of an image line is reached
x_in	1	Out	New value for the x-mask
y_in	1	Out	New value for the y-mask
Valid	1	Out	Is the current pixel valid at all (within the image limits)?

Tab. 14

Signal	Bits	Type	Description
EN	1	In	Enable signal of the module
Win_p	289	In	Positively marked pixel in the edge window
Win_n	289	In	Negatively marked pixel in the edge window
xmask	17	In	x-mask (validity of the pixels in the edge window)
ymask	17	In	y-mask (validity of the pixels in the edge window)
yReal	16	Out	Position of the straight line with respect to the color jump
mix	7	Out	Mix factor which specifies how much of the color from the corresponding direction is to be mixed (if only that straight line exists)
len	5	Out	Horizontal length of the traced straight line
nogood	1	Out	Flag which specifies whether the straight line is deemed "good"

Tab. 15

Signal	Bits	Type	Description
actWin_p	289	In	Positively marked pixels in the edge window
actWin_n	289	In	Negatively marked pixels in the edge window
xmask	17	In	Validity of the pixels in the window
ymask	17	In	Validity of the lines in the window
maskedWindow	191	Out	Masked edge window

Tab. 16

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
ep	191	In	Edge window (edge pic/no longer rectangular)
stat_left	2	Out	Status at the left end of the traced step
stat_right	2	Out	Status at the right end of the traced step
xA	4	Out	x-value of the start point (actually -xA but sign is not required/value range:0..7.5)
yA	5	Out	y-value of the start point (value range:-7.5..+7.5)
xE	4	Out	x-value of the end point (value range:0..7.5)
yE	5	Out	y-value of the end point (value range: -7.5..+7.5)

Tab. 17

Signal	Bits	Type	Description
up	9	In	Line in the edge image above the middle one
center	9	In	Middle line in the edge image in one direction
down	9	In	Line in the edge image below the middle one
len	3	Out	Length of the central step in the traced direction
stat	3	Out	Status at the end of the central step

Tab. 18

Signal	Bits	Type	Description
tstat_l	3	In	Temporary status towards the left
tstat_r	3	In	Temporary status towards the right
stat_l	2	Out	Status at the left end of the traced step
stat_r	2	Out	Status at the right end of the traced step

Tab. 19

tstat	Bits(2:0)
UP	010
DOWN	001
NO	000
HOR	011
BOTH	100

Tab. 20

stat	Bits(1:0)
UP	10
DOWN	01
NO	00
HOR	11

Tab. 21

Signal	Bits	Type	Description
pos	3	In	Position at which the central step ends
ep	44	In	Sector from the edge image in which further steps are to be found
jumps	17	Out	Jumps found in the sector

Tab. 22

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
stat_l	2	In	Status at the left edge of the central step
stat_r	2	In	Status at the right edge of the central step
pos_l	3	In	Length of the central step towards the left
pos_r	3	In	Length of the central step towards the right
jumps_l	17	In	Further steps recognised towards the left
jumps_r	17	In	Further steps recognised towards the right
xA	4	Out	x-value of the start point
yA	4	Out	y-value of the start point (without sign)
xE	4	Out	x-value of the end point
yE	4	Out	y-value of the end point (without sign)

Tab. 23

Signal	Bits	Type	Description
len	4	In	Length of the central step
jumps	17	In	Possible jumps
pos	7	Out	Mask which specifies which steps include a length greater by one than the central step
zero	7	Out	Mask which specifies which steps contain the same length as the central step
neg	7	Out	Mask which specifies which steps contain a length shorter by one than the central step

Tab. 24

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
pos_l	7	In	Mask which contains the steps longer by one towards the left
zero_l	7	In	Mask which contains the steps of the same length towards the left
neg_l	7	In	Mask which contains the steps shorter by one towards the left
pos_r	7	In	Mask which contains the steps longer by one towards the right
zero_r	7	In	Mask which contains steps of the same length towards the right
neg_r	7	In	Mask which contains the steps shorter by one towards the right
mask_l	7	Out	Mask which specifies which steps towards the left contribute to a straight line
mask_r	7	Out	Mask which specifies which steps towards the right contribute to a straight line

Tab. 25

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
pos	3	In	x-value of the end of the central step
y0	1	In	y-value of the end of the central step
jumps	17	In	Further steps in the corresponding direction
mask	7	In	Mask which specifies which of the steps in jumps contribute to the straight line
x	4	Out	x-value of the one end point of the straight line
y	4	Out	Magnitude of the y-value of the one end point of the straight line

Tab. 26

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
xA	4	In	x-value of the start point
yA	5	In	y-value of the start point
xE	4	In	x-value of the end point
yE	5	In	y-value of the end point
stat_left	2	In	Status at the start point
stat_right	2	In	Status at the end point
yReal	16	Out	y-value of the real straight line in the current pixel
mix	7	Out	Mixed factor for a mixing direction rel. to the straight line
len	5	Out	Length of the traced straight line
no_good	1	Out	Statuses at the ends of the straight line indicate not a "benign" straight line

Tab. 27

Signal	Bits	Type	Description
x	5	In	Input value
y	10	Out	Input value = $\frac{1}{x}$

Tab. 28

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
xmask	1	In	Mask bit which specifies whether the current pixel belongs to an edge
yReal	16	In	y-value of the real edge relative to the color jump
len_r	5	In	Length of the traced straight line for the right mix factor
nogood_r	1	In	Flag indicating that the straight line was probably not "benign" for ascertaining the right mix factor
mix	7	Out	Left mix factor for the current pixel
len	5	Out	Length of the traced straight line
nogood	1	Out	Statuses at the end of the straight line indicate not a "benign" straight line

Tab. 29

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
pre_mix_up, pre_mix_down, pre_mix_left, pre_mix_right	je 7	In	Mix factors which were established on the basis of only one respective straight line
len_up, len_down, len_left, len_right	je 5	In	Lengths of the respective straight line
nogood_up, nogood_down, nogood_left, nogood_right	je 1	In	Flags of the respective straight lines which cannot be deemed "good"
mix_up, mix_down, mix_left, mix_right	je 7	Out	Definitive mixing factors for the corresponding directions

Tab. 30

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
mix_up, mix_down, mix_left, mix_right	je 7	In	Mix factors for the corresponding directions
col_up	24	In	Color of the pixel above the current one
col_right	24	In	Color of the pixel to the right of the current one
col_down	24	In	Color of the pixel below the current one
mixedColor	24	Out	New color of the current pixel by virtue of mixing
mixing	1	Out	Flag whether mixing occurred (in triple buffer mode the decision whether the pixel has to be written back)
col_up_new	24	Out	Color which is used in the next line as uppermost pixel
col_right_new	24	Out	Color which is used in the next line as right pixel

Tab. 31

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
mix_up, mix_down, mix_left, mix_right	je 7	In	Mix factors for the corresponding directions
mix_u, mix_d, mix_l, mix_r	je 7	Out	Mix factors delayed by one cycle
mix_c	7	Out	Central mix factor
shift	1	Out	Flag whether the mixed factors must still all be divided by two
mixing	1	Out	Flag whether mixing occurs or whether the central factor is 1.0

Tab. 32

Signal	Bits	Type	Description
EN	1	In	Enable signal of the registers
mix_u, mix_d, mix_l, mix_r, mix_c	je 7	In	Mix factors for the corresponding pixels
col_u, col_d, col_l, col_r, col_c	je 8	In	Colors of the individual pixels in the respective color channel
shift	1	In	Flag that division must still occur by 2
mixedColor	8	Out	Mixed color for the color channel

Tab. 33